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(54) Abstract Title

Dual mode master/slave system on IC

(57) A scalable processor independent bus is disclosed. Each bus master function block is provided with a bus master interface having a state machine that implements at least two operational modes, including a two state fast mode, and an at least four state normal mode. Each bus slave function block is likewise provided with a bus slave interface having a state machine that implements the two operational modes in a complementary manner. Each bus master/slave function block is provided with a bus master/slave interface having a state machine that implements the at least two operational modes in the role of a bus master as well as in the role of a bus slave. Each bus master, slave, or master/slave interface is equipped to facilitate scaling of the address as well as data width. In various embodiments of the present invention, they are equipped to support multiple masters on the bus, broadcast writes, burst mode transfers, and/or tri-states.

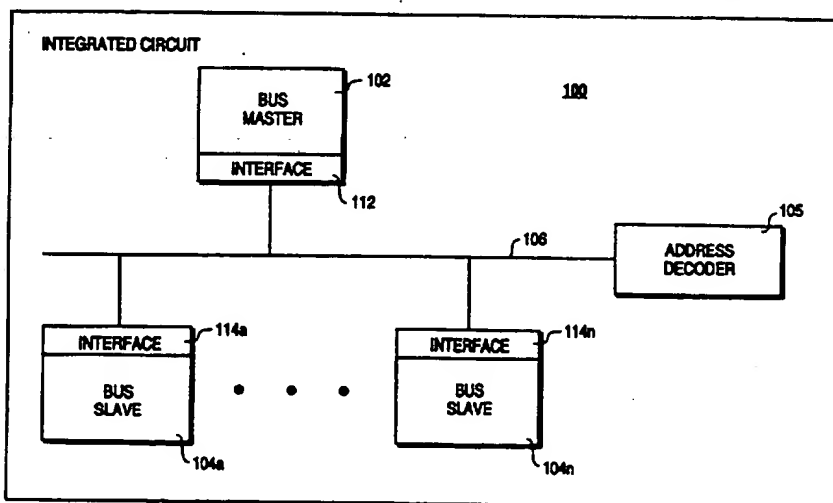


FIG. 1

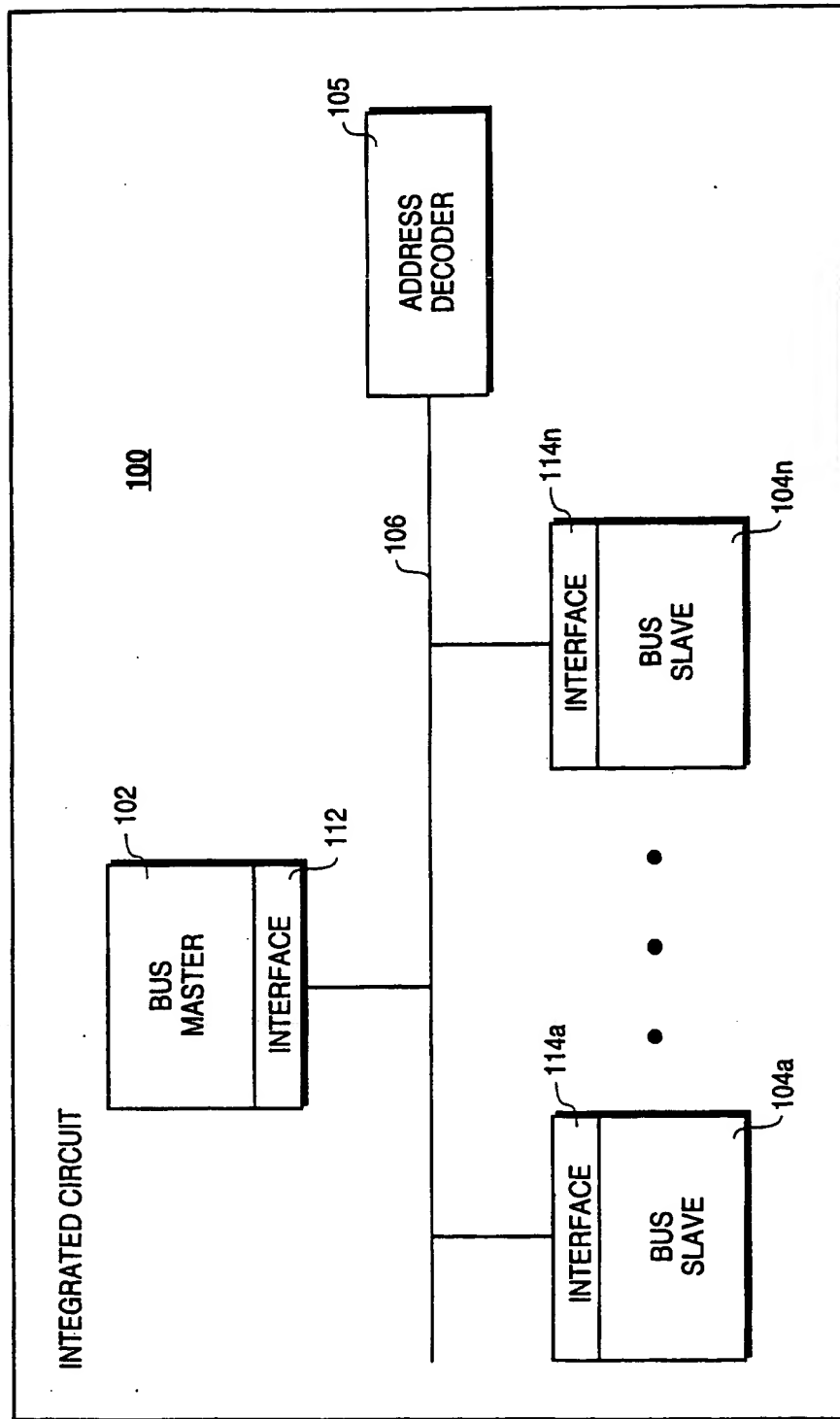
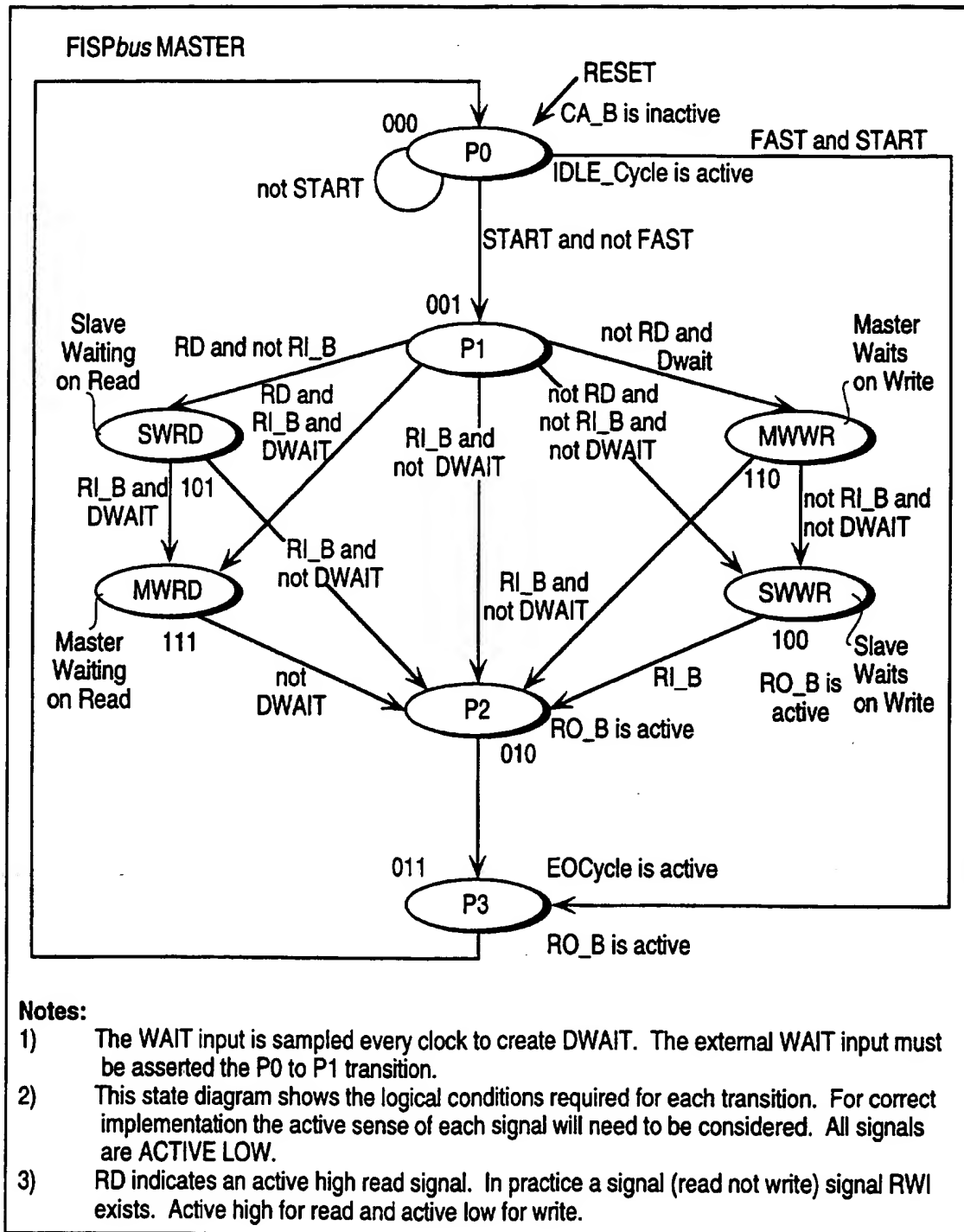
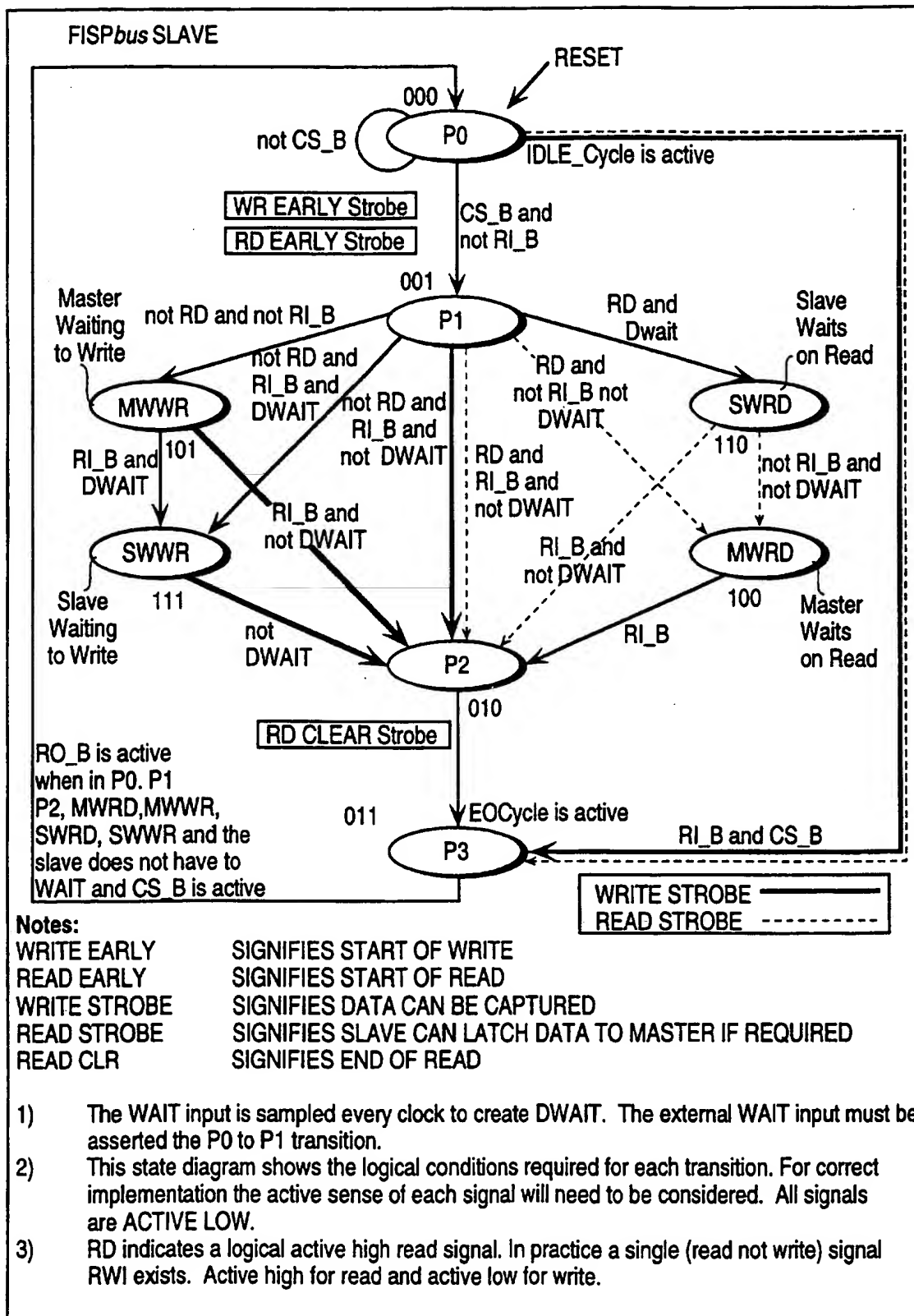


FIG. 1

**FIG. 2**

**FIG. 3**

NAME	M/S	I/O	DESCRIPTION
RESET	Master and Slave	IN	Active Low reset signal. Forces interface to reset condition.
FAST	Master	IN	Active Low mode signal to enable fast two cycle bus accesses, asserted at the P0 state.
START	Master	IN	Active Low start Master bus cycle signal. Ignored by the slave.

FIG. 4

NAME	M/S	I/O	DESCRIPTION
WAIT	Master and Slave	IN Ctrl Line	Active Low signal indicating the module requires more than 4 cycles for an access. Wait cycles are inserted while this signal is active. Note: This signal is internally latched and takes 1 clock to take effect, therefore, it is first asserted while in the P0 state.
RWI	Master and Slave	IN from Bus (S) IN Ctrl Line (M)	Read / Write line. A high indicates a read cycle and low a write operation. When in Master mode this line indicates the type of access required. When in Slave mode this line indicates type of access in progress.
CS_B	Slave	IN from Bus (S)	Active Low chip select signal that indicates that the current access is for this module.
RI_B	Master and Slave	IN from Bus (M) IN from Bus (S)	Active Low Ready in handshake signal. To a Master a low input indicates that the target slave is ready. To a slave an active low indicates that the Master is ready. A simultaneous low on this signal and the CS_B indicates a FAST access to a Slave
RO_B	Master and Slave	OUT to Bus	Active Low Ready out handshake signal. The RO_B from the active master is routed to all slaves as the slave RI_B. The Output from all slaves are ANDED together and returned to the Master as its RI_B.
CA_B	Master	OUT to Bus	Active Low Cycle Active signal indicates an active cycle in progress. The Master generated signal is connected to the appropriate Slave after decoding the Slaves base address.
EOCycle	Master and Slave	OUT	Active Low End of Cycle indication. i. e. state machine is in P3.
IDLE_Cycle	Master and Slave	OUT	Active Low Idyl Cycle indication. i. e. state machine is in P0.

FIG. 5

NAME	M/S	I/O	DESCRIPTION
Rd_Early_B	Slave	OUT	Active Low strobe indicating an early read can take place. Used to activate an action before a read. Not supported in fast mode.
Wr_Early_B	Slave	OUT	Active Low strobe indicating an early write can take place. Used to activate an action before a write. Not supported in fast mode.
Rd_Clr_B	Slave	OUT	Active Low strobe indicating a late read can take place. Used to activate an action after a read or to clear the data after a read. Not supported in fast mode.
Rd_Stb_B	Slave	OUT	Active Low strobe indicating a read is taking place. This is the normal read strobe.
Wr_Stb_B	Slave	OUT	Active Low strobe indicating a write can take place. This is the normal write strobe position.

FIG. 6

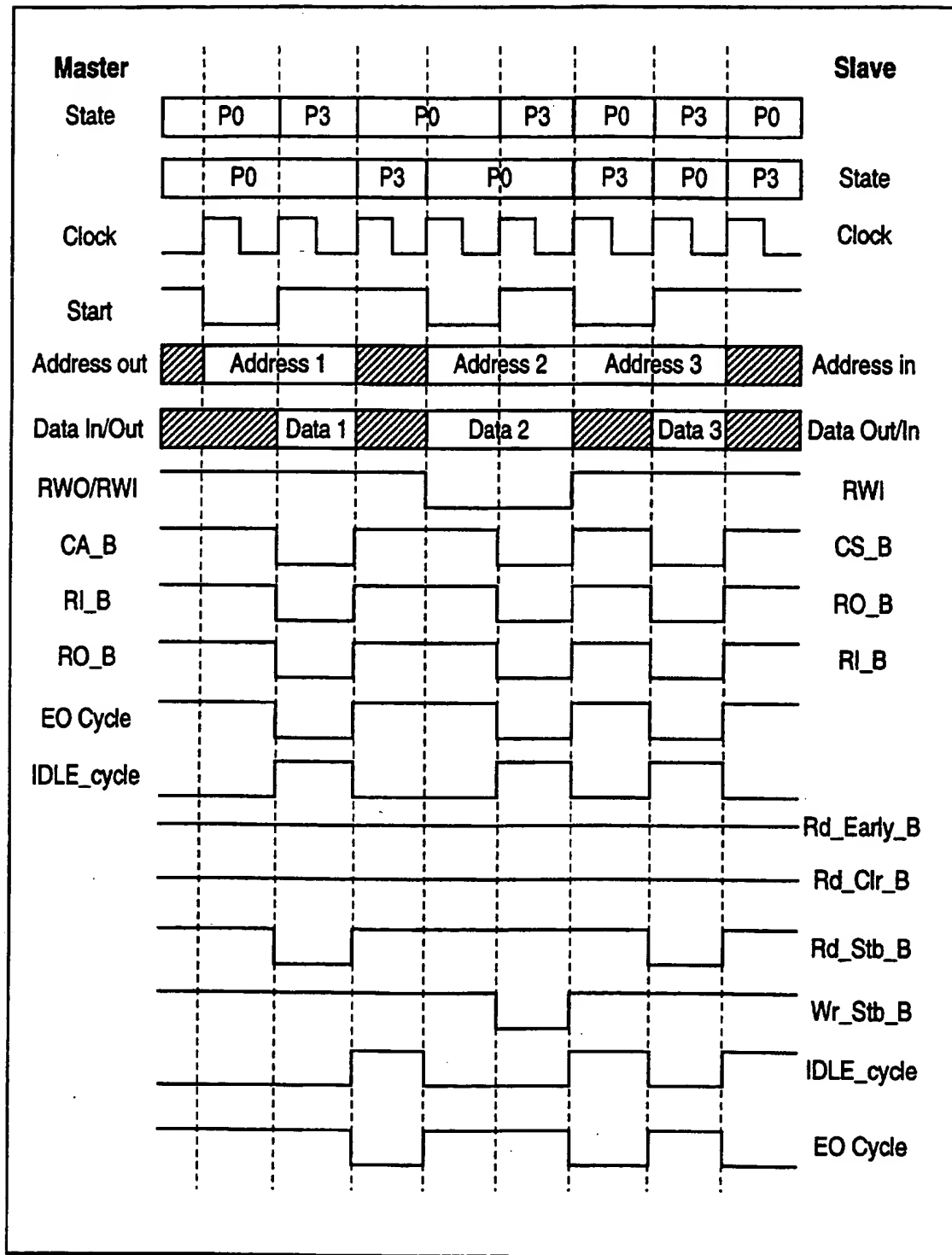


FIG. 7

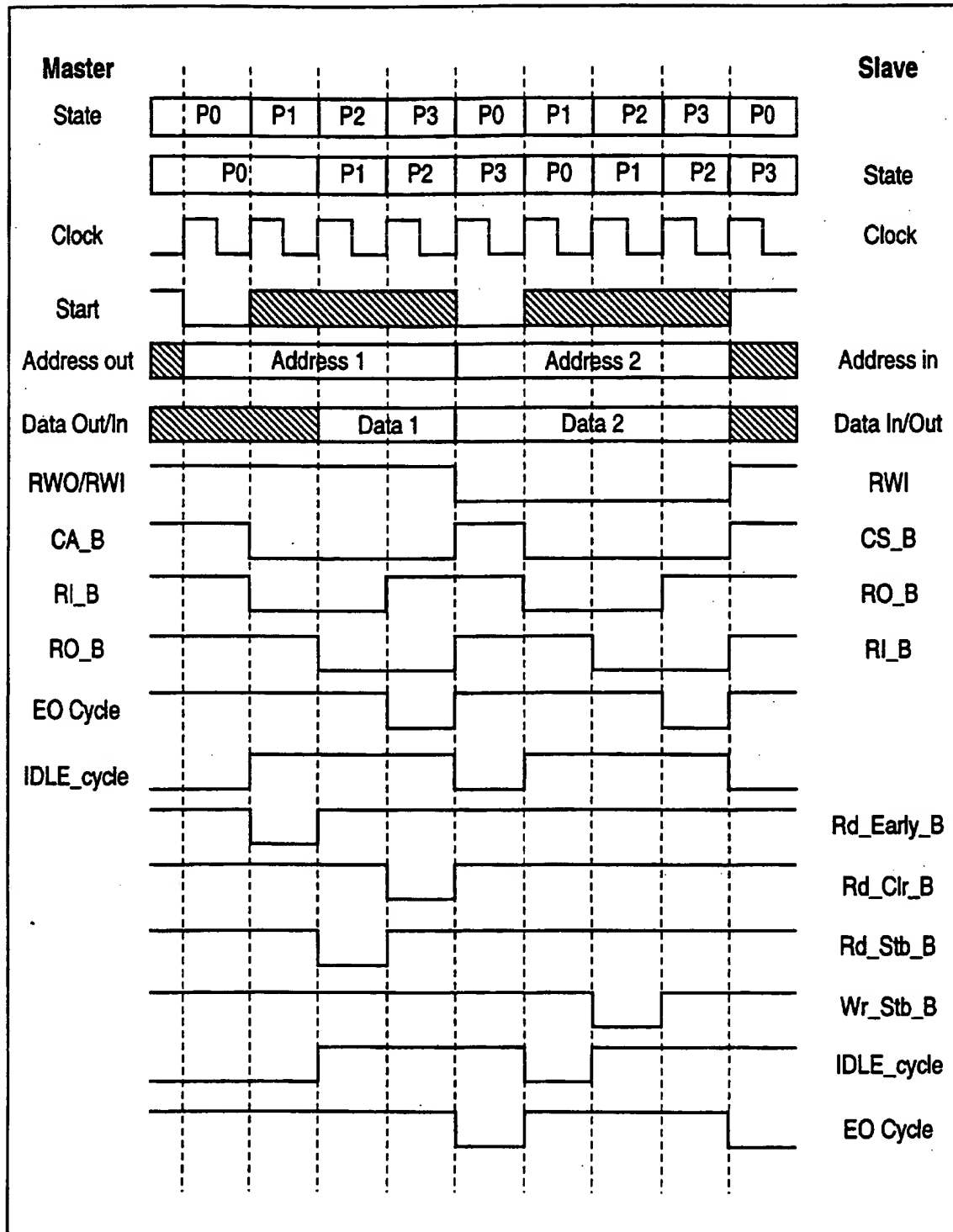


FIG. 8

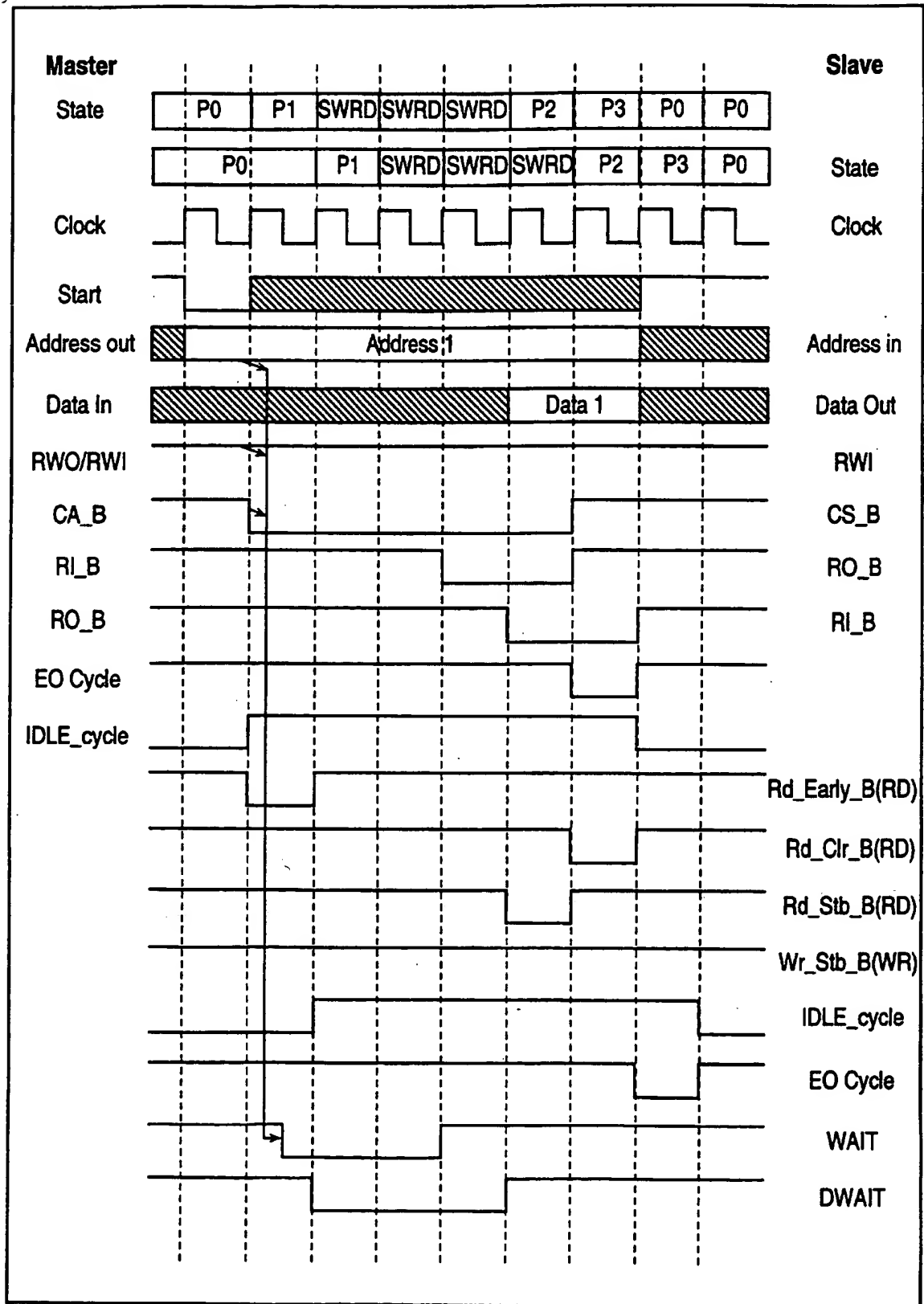


FIG. 9

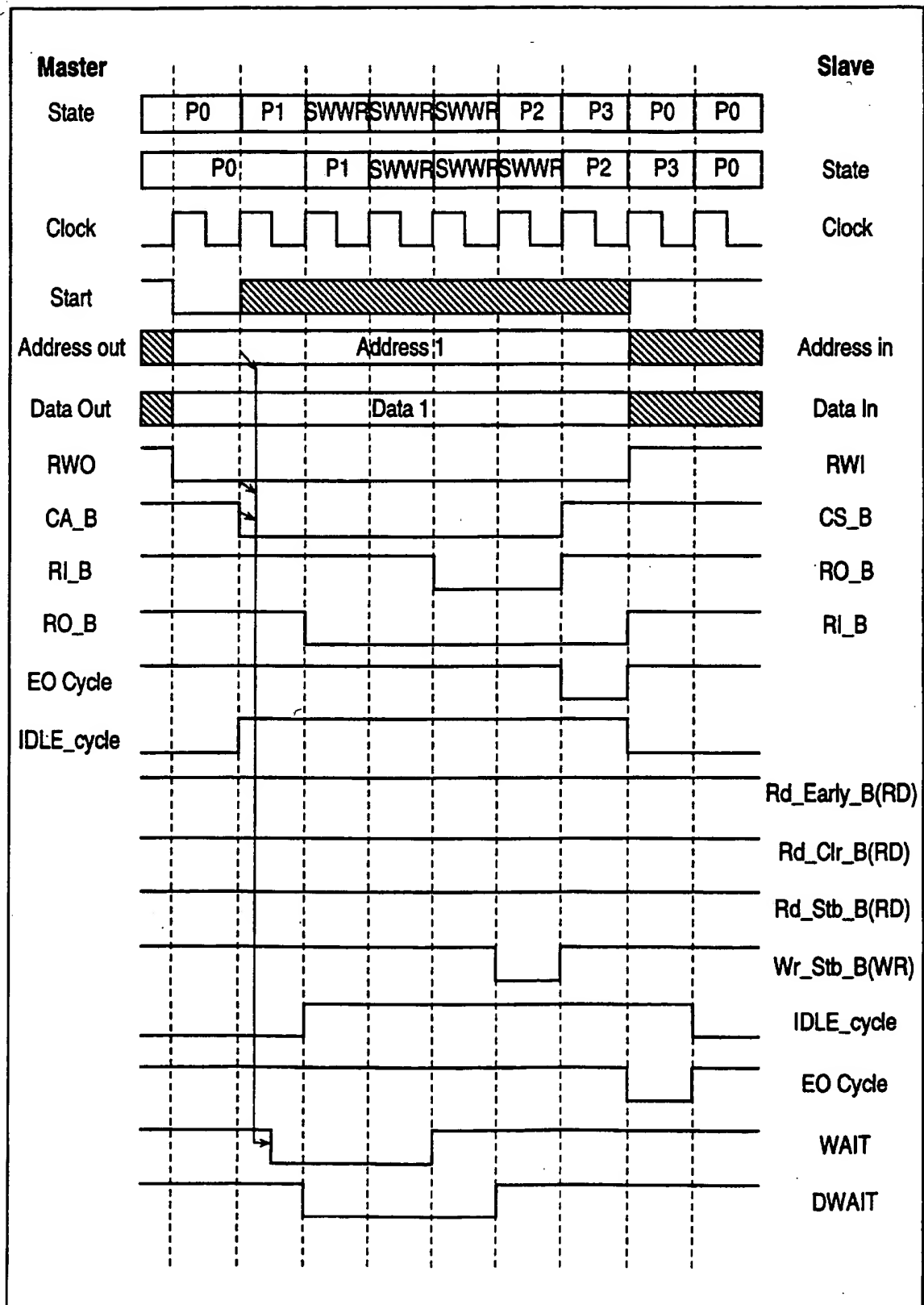


FIG. 10

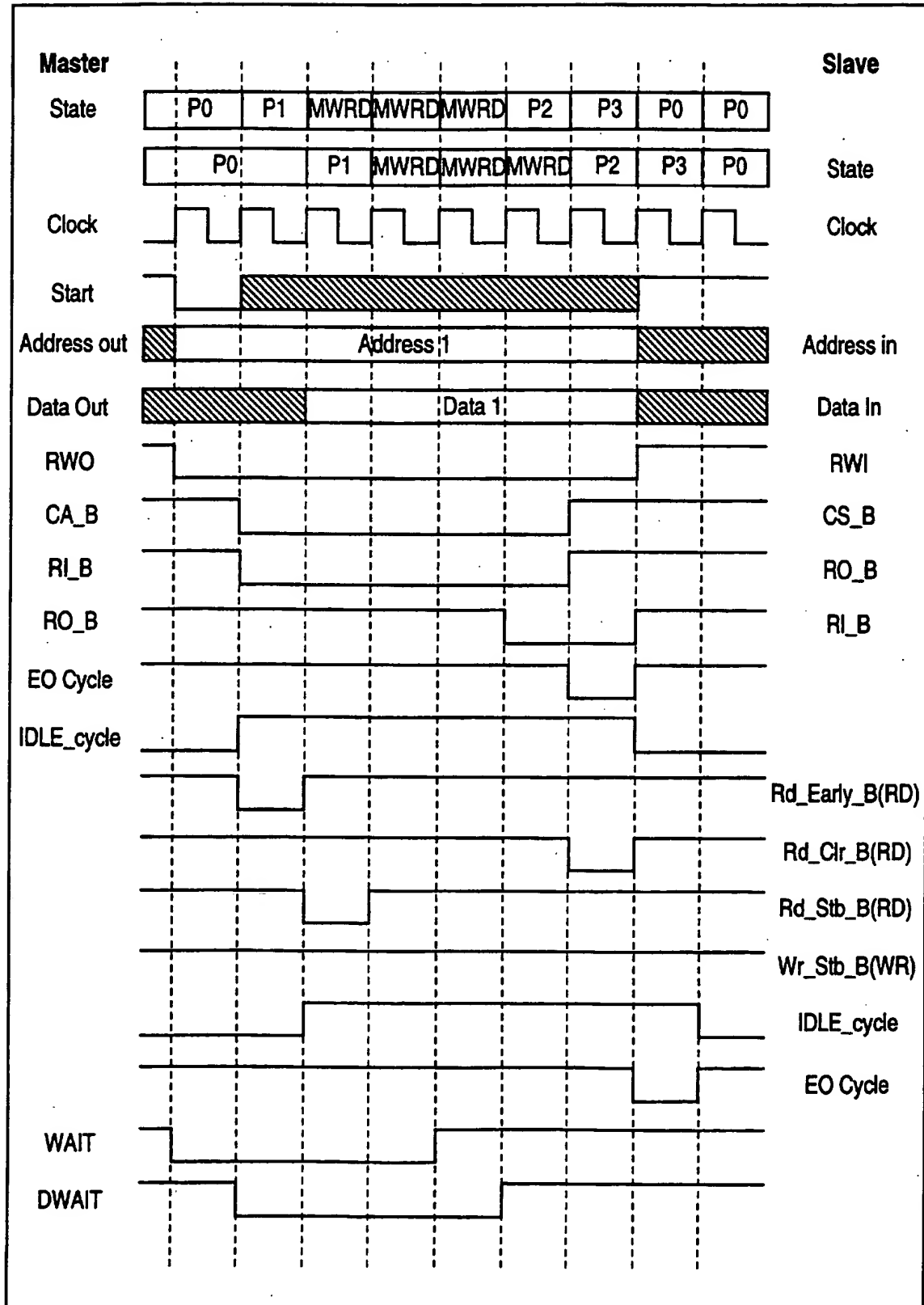


FIG. 11

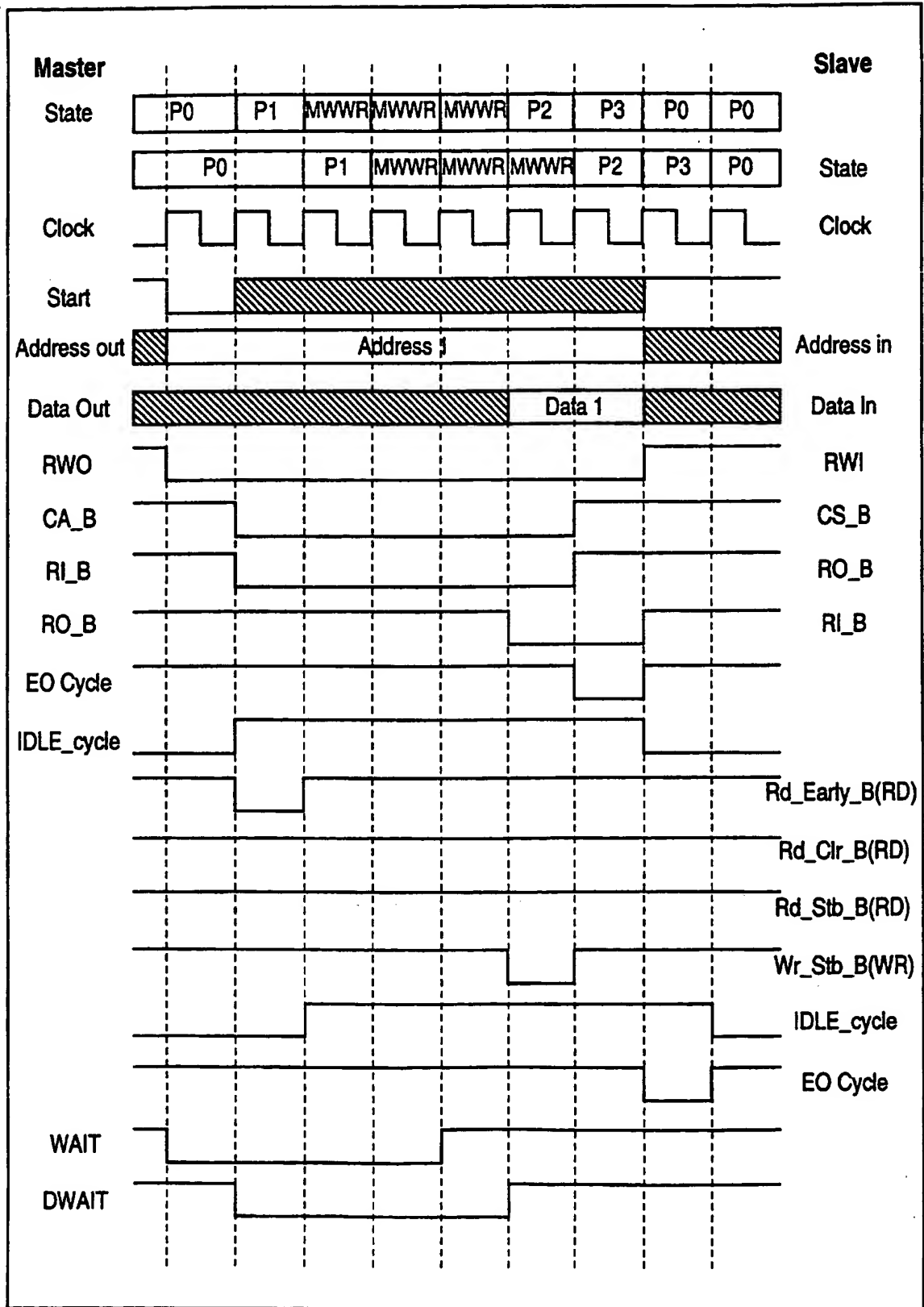


FIG. 12

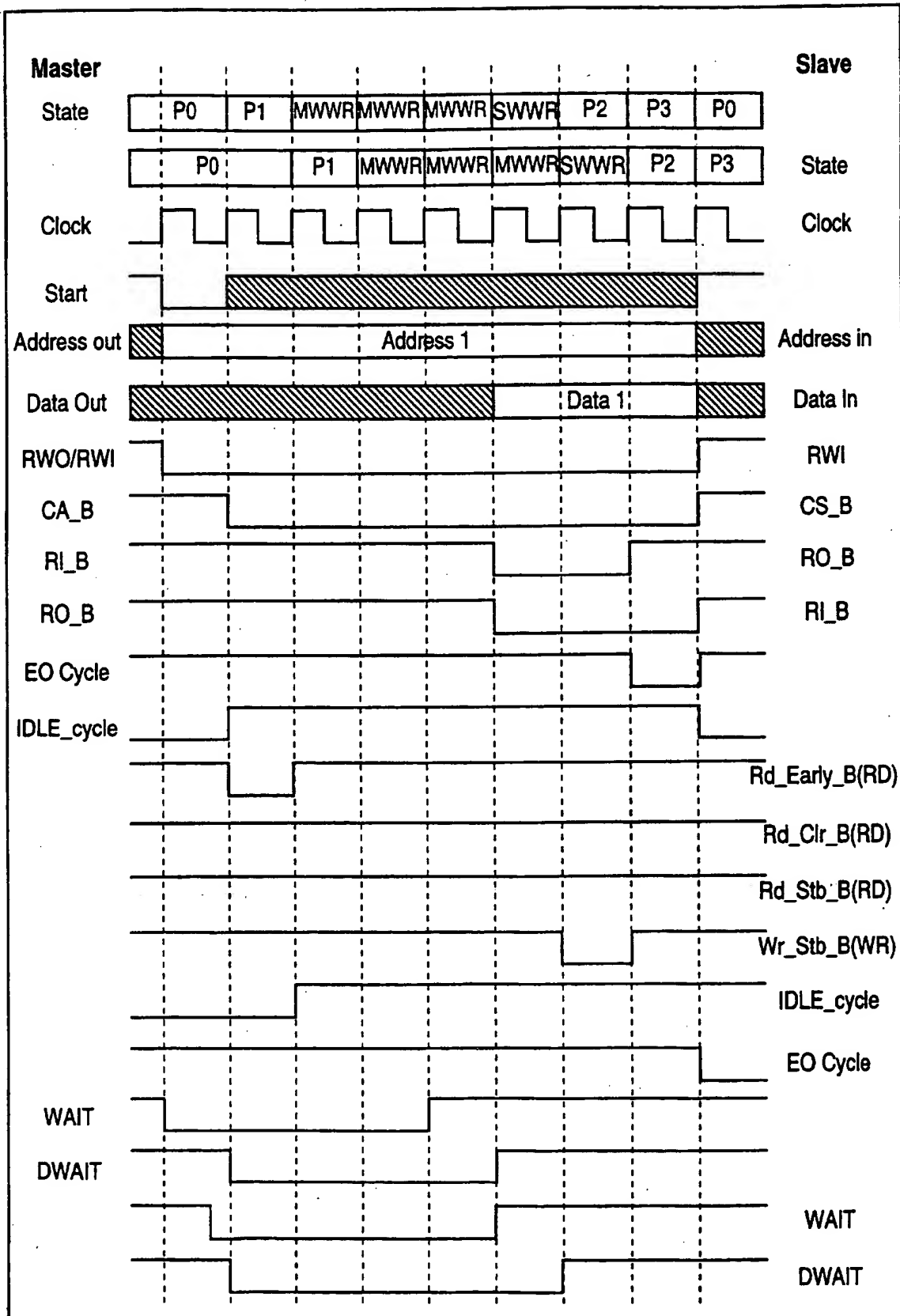


FIG. 13

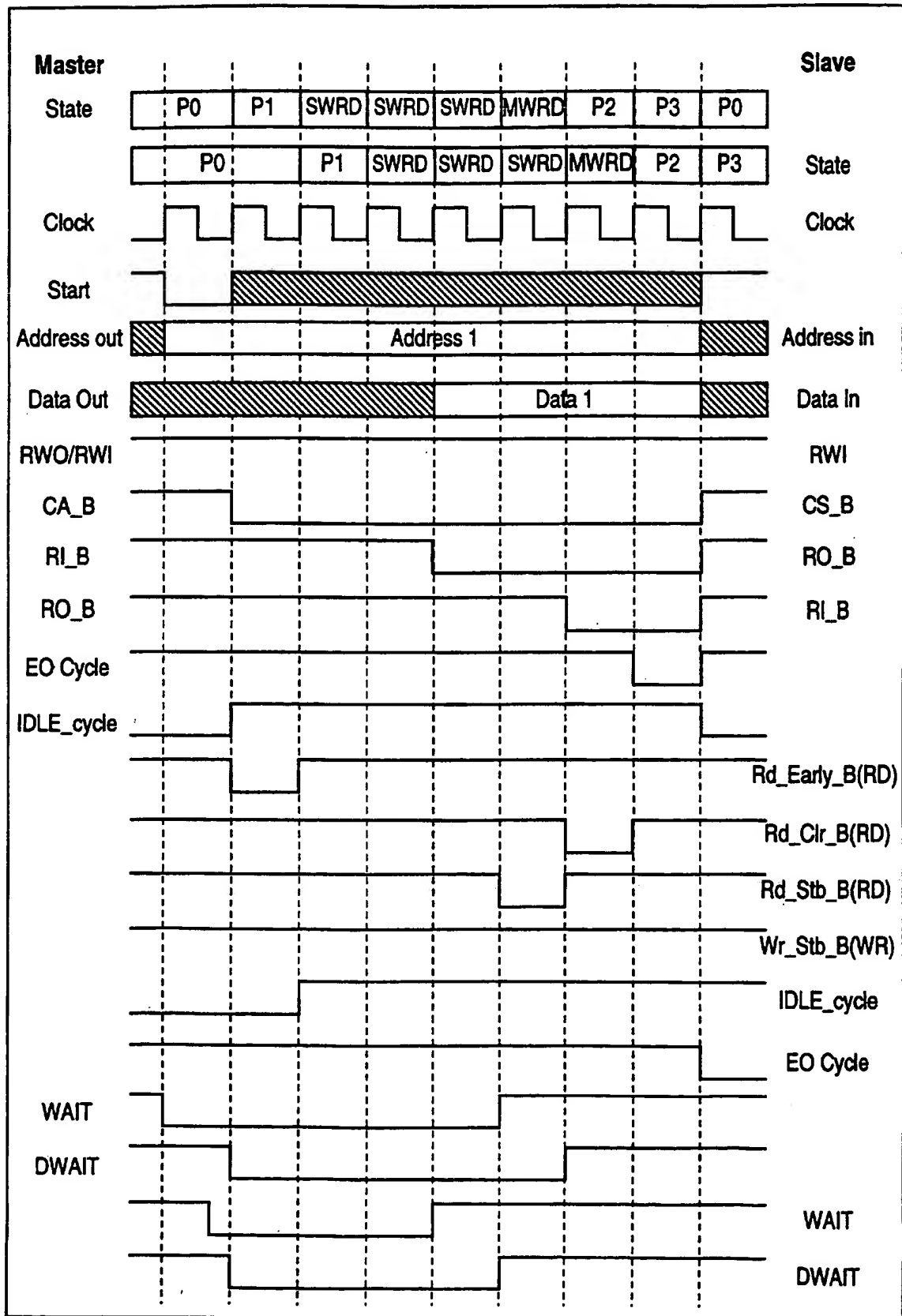


FIG. 14

Additional Fispbus Signals		
Name	Size	Description
MMG	1	Active Low Master Mode Grant signal. This signal originates in the Fispbus arbiter and starts the Master operation.
MMR	1	Active High Master Mode Request signal. This signal requests bus ownership from the Fispbus arbiter and ownership is granted by MMG.
CA_B	Number of bytes in data width + 1	Output Bus of active low "chip selects". Bit 0 is the AND of all chip selects with Bit 1 to N indicating individual byte selects with bit 1 corresponding to the LSB and bit N corresponding to the MSB.

FIG. 15

Additional Fispbus Signals		
Name	Size denoted	Description
AI	Fispbus Address Width	Address in from the current Master. The minimum size of this bus is determined by the maximum address range required by the Slaves on the bus. The current Master is determined by the bus arbiter.
CS_B	Number of Bytes in Data Width +1	Bus of active low "chip selects". Bit 0 is the AND of all chip selects with Bit 1 to N indicating individual byte selects with bit 1 corresponding to the LSB and bit N corresponding to the MSB.
FTS	1	Active Low Free to Send signal. A low on this signal will indicate to the arbiter that the Slave has data to be read. Removal of this signal must take place within P0 before any transition to the next state. Use of this signal is not mandatory.
FTR	1	Active High Free to Receive signal. A high on this signal will indicate to the arbiter that the Slave has room to receive data. Removal of this signal must take place within P0 before any transition to the next state. Use of this signal is not mandatory.
IG	Number of interrupts in Module +1	Active low interrupt Grant lines. Bit 0 is the AND of all interrupt grants to this module and bits 1-N are individual grants for each interrupt within the block. Support of interrupt grants beyond 0 is not mandatory and is only required for vectored interrupts.
DO	Fispbus Data Width	Data out from the Slave. The minimum size of this bus is determined by the maximum data range required by the Slaves on the bus. The Data out from each Slave module is multiplexed by the bus arbiter to create the common Fispbus data bus.
DI	Fispbus Data Width	Data in from the Master. The minimum size of this bus is determined by the maximum data range required by the Slaves on the bus. This is the common Fispbus data bus.
IR	Number of interrupts in module +1	Active low Interrupt Request lines. Bit 0 is the AND of all interrupt requests from this module and bits 1-N are individual requests for each interrupt within the block. Support of interrupt requests beyond 0 is not mandatory and is only required for vectored interrupts.

FIG. 16

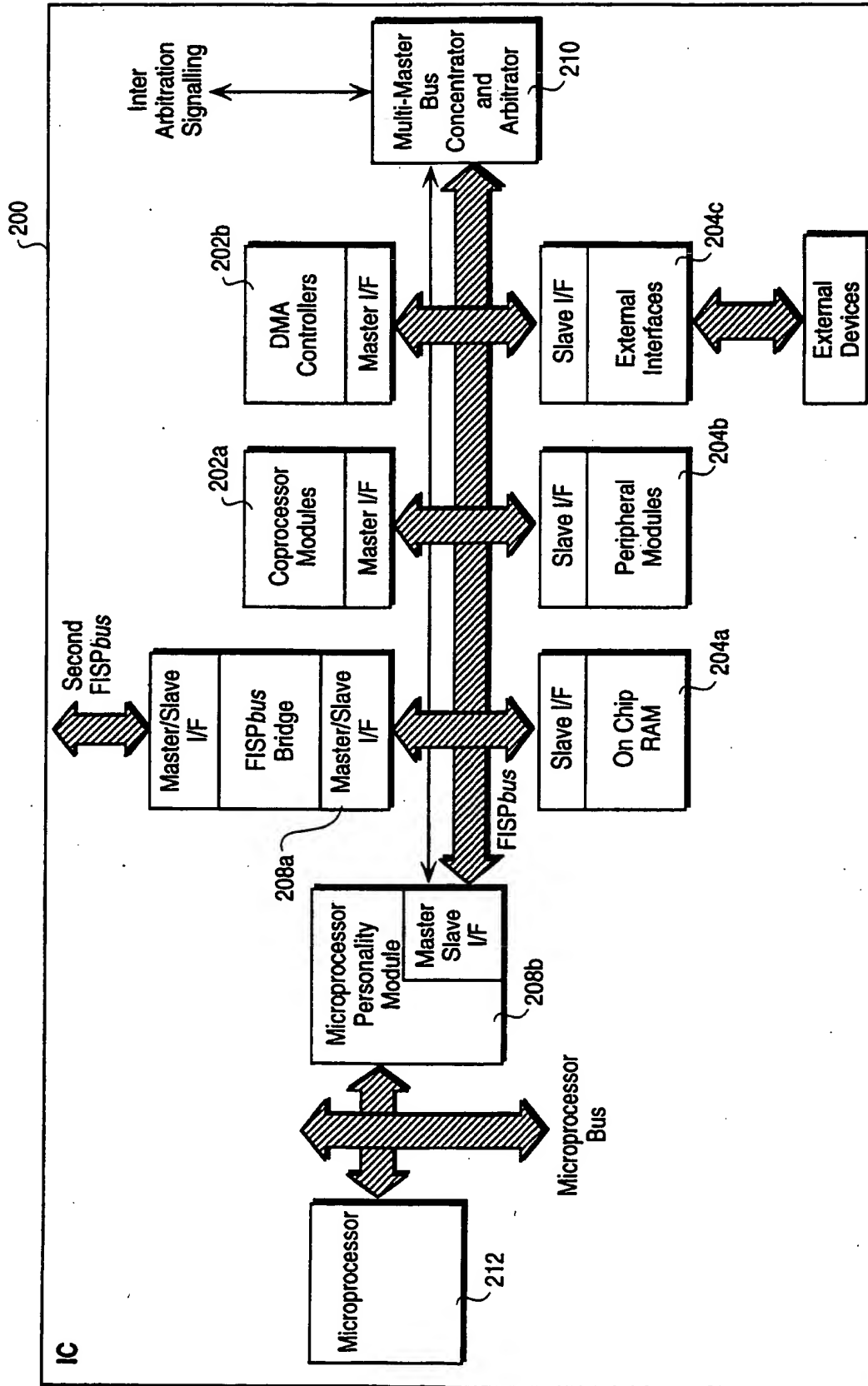
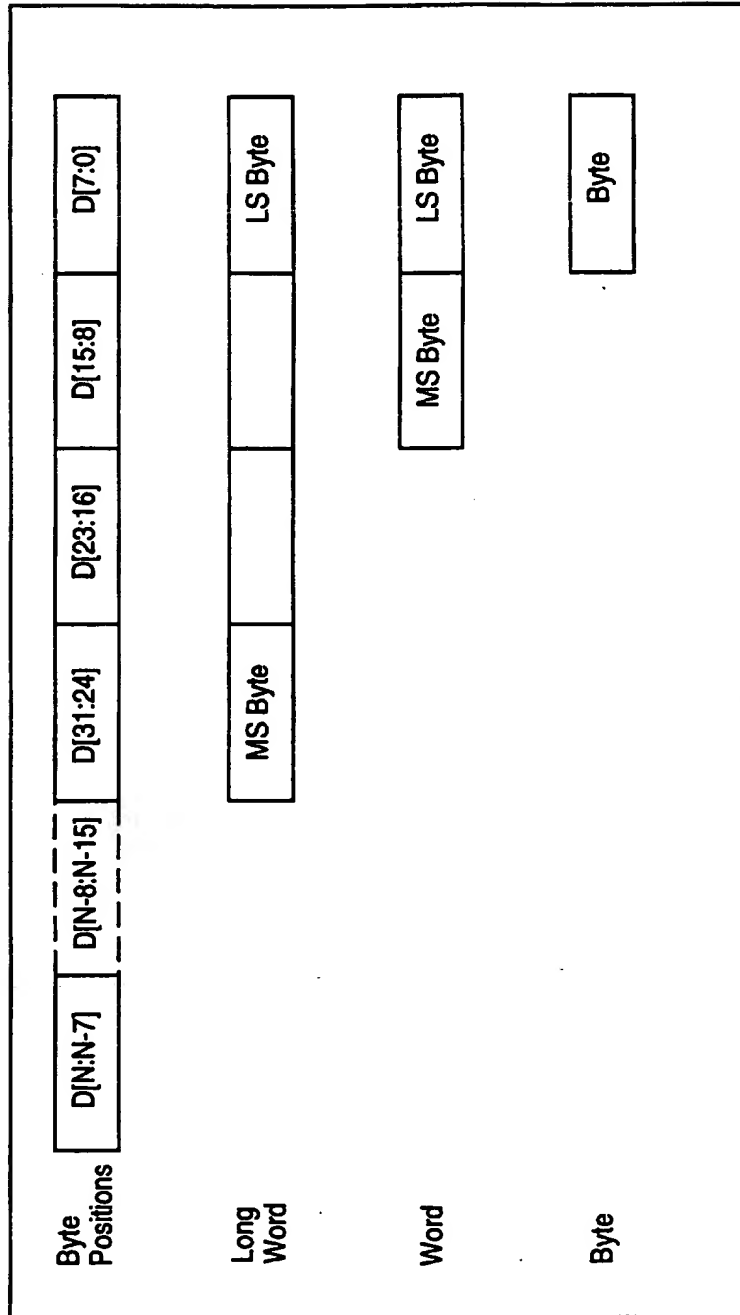


FIG. 17

**FIG. 18**

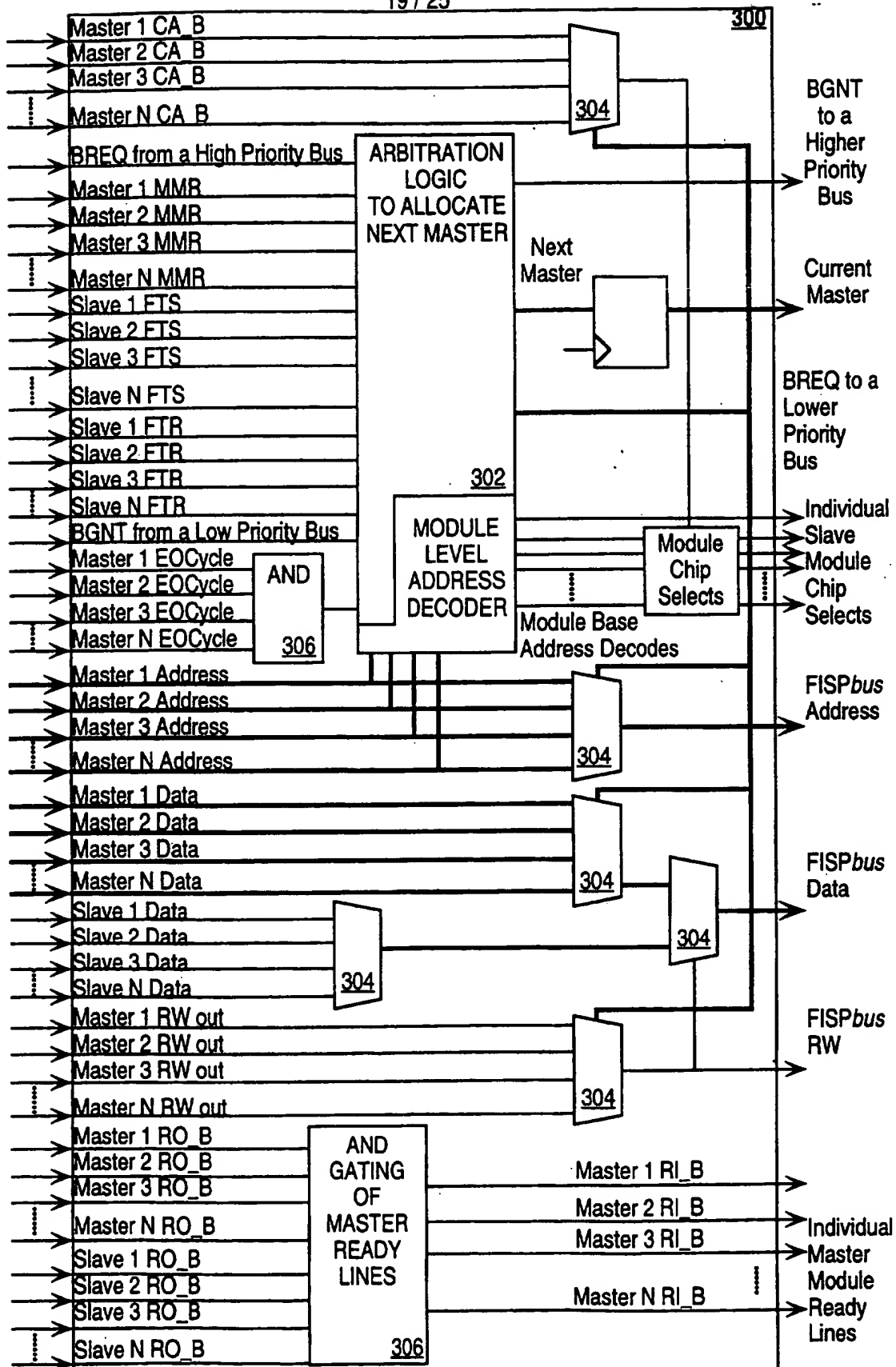


FIG. 19

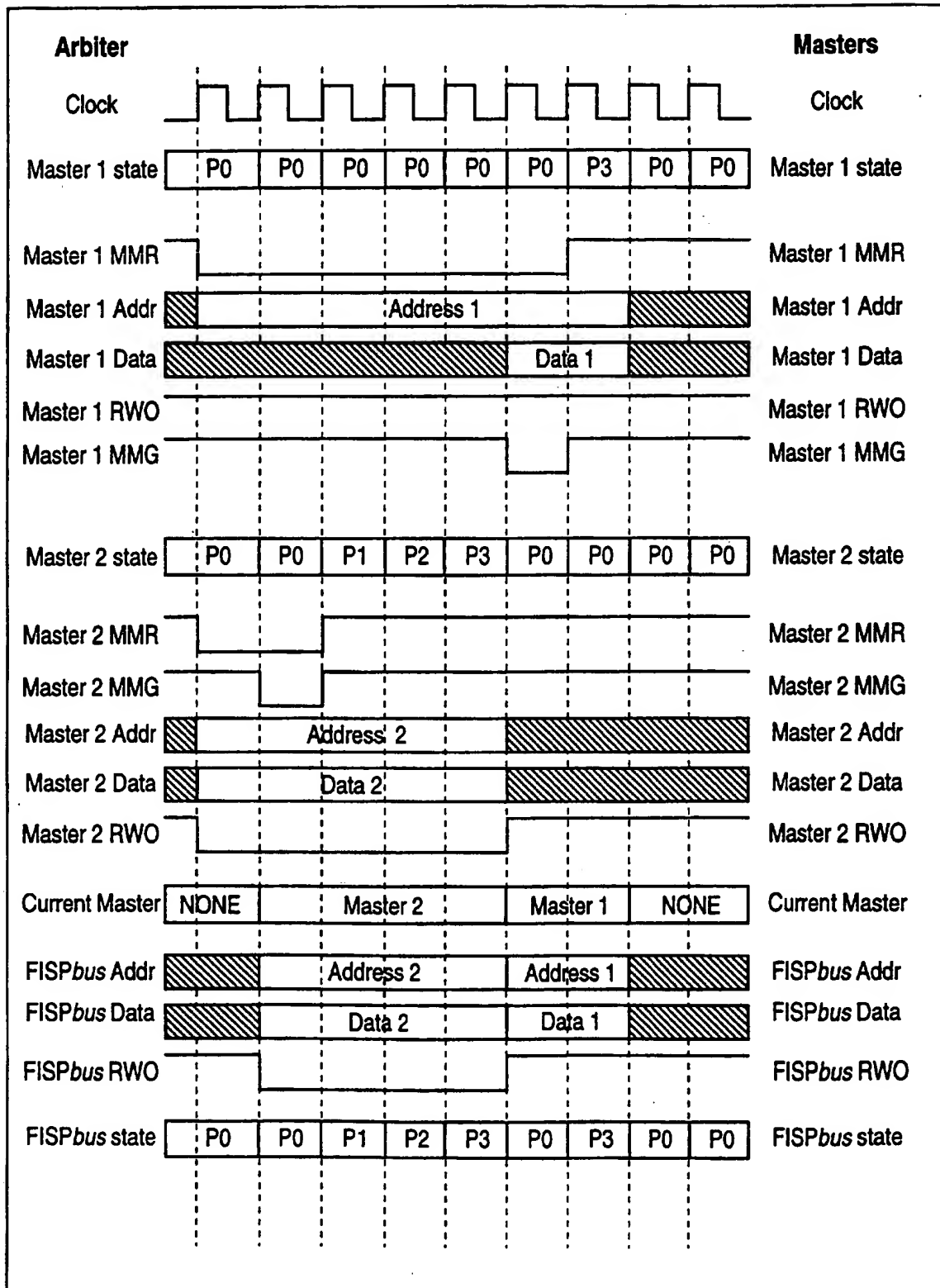


FIG. 20

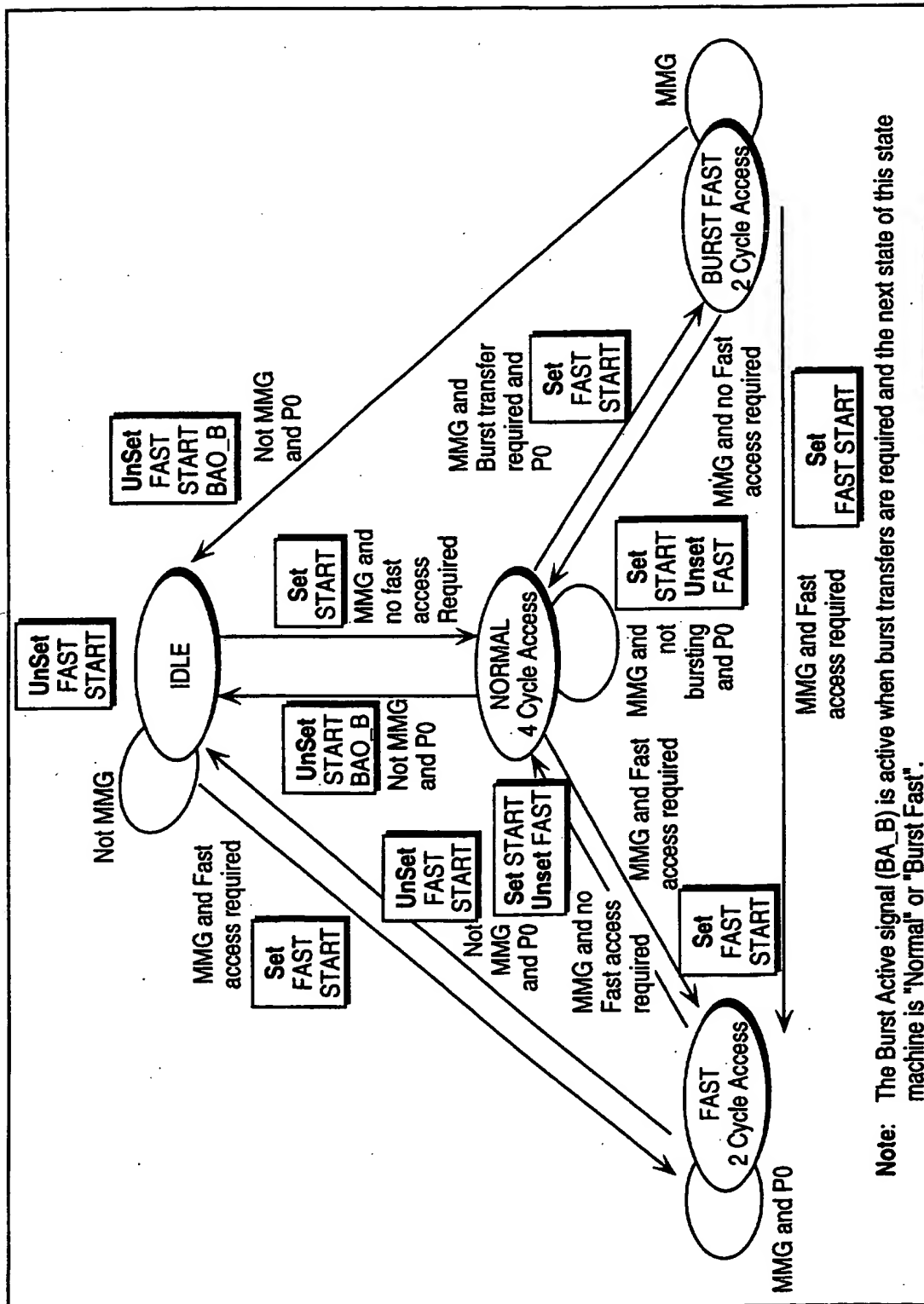


FIG. 21

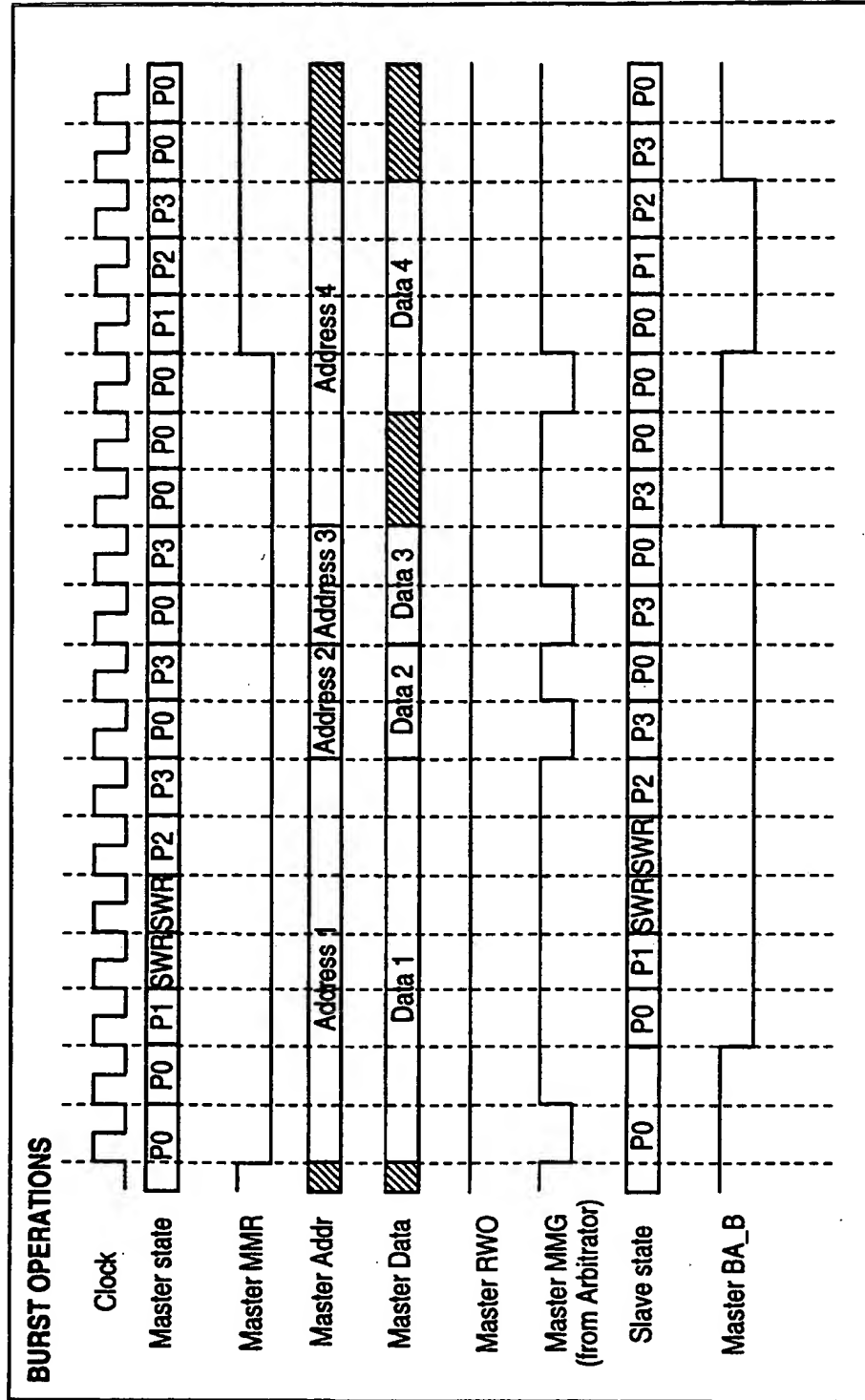


FIG. 22

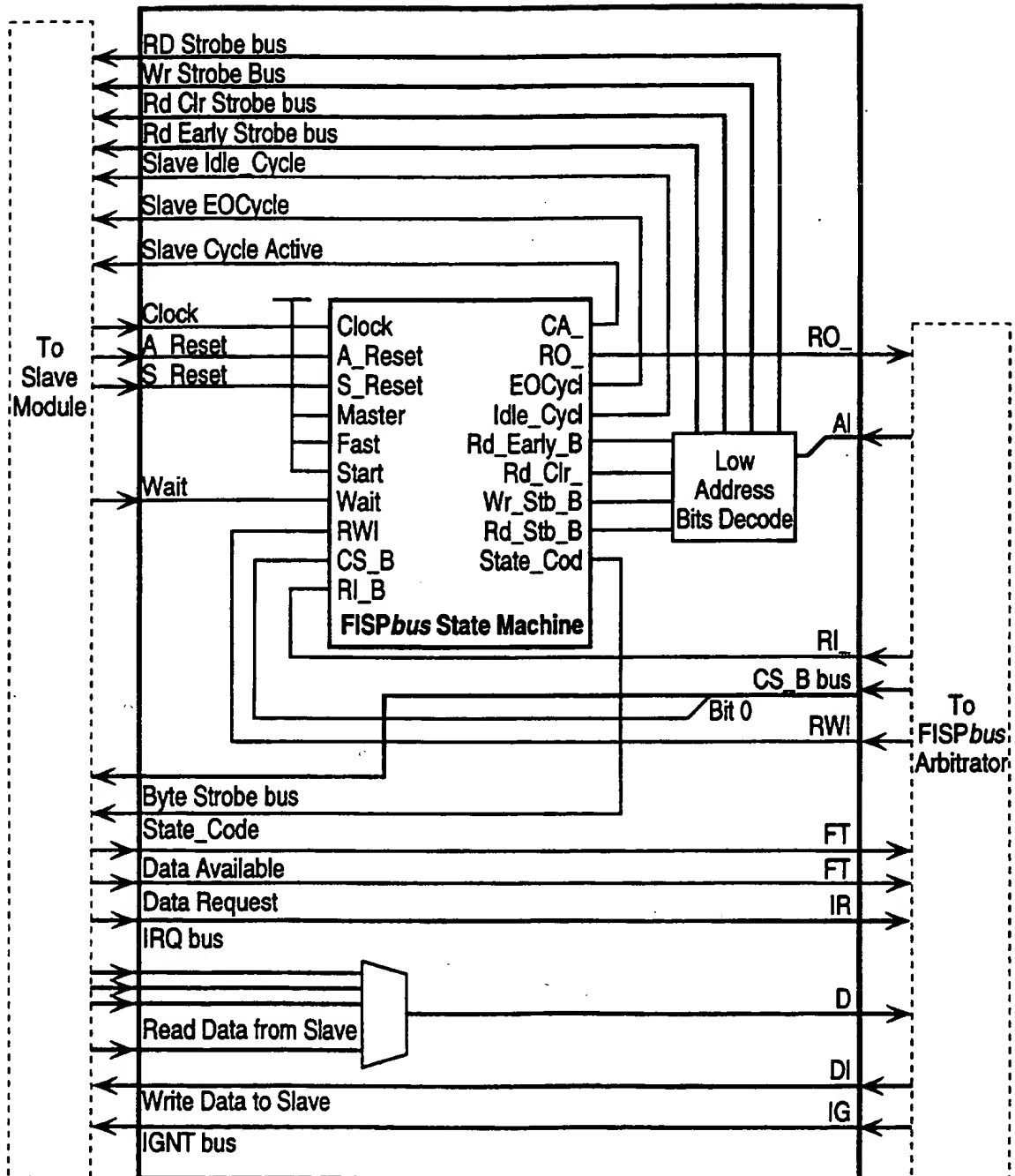


FIG. 23

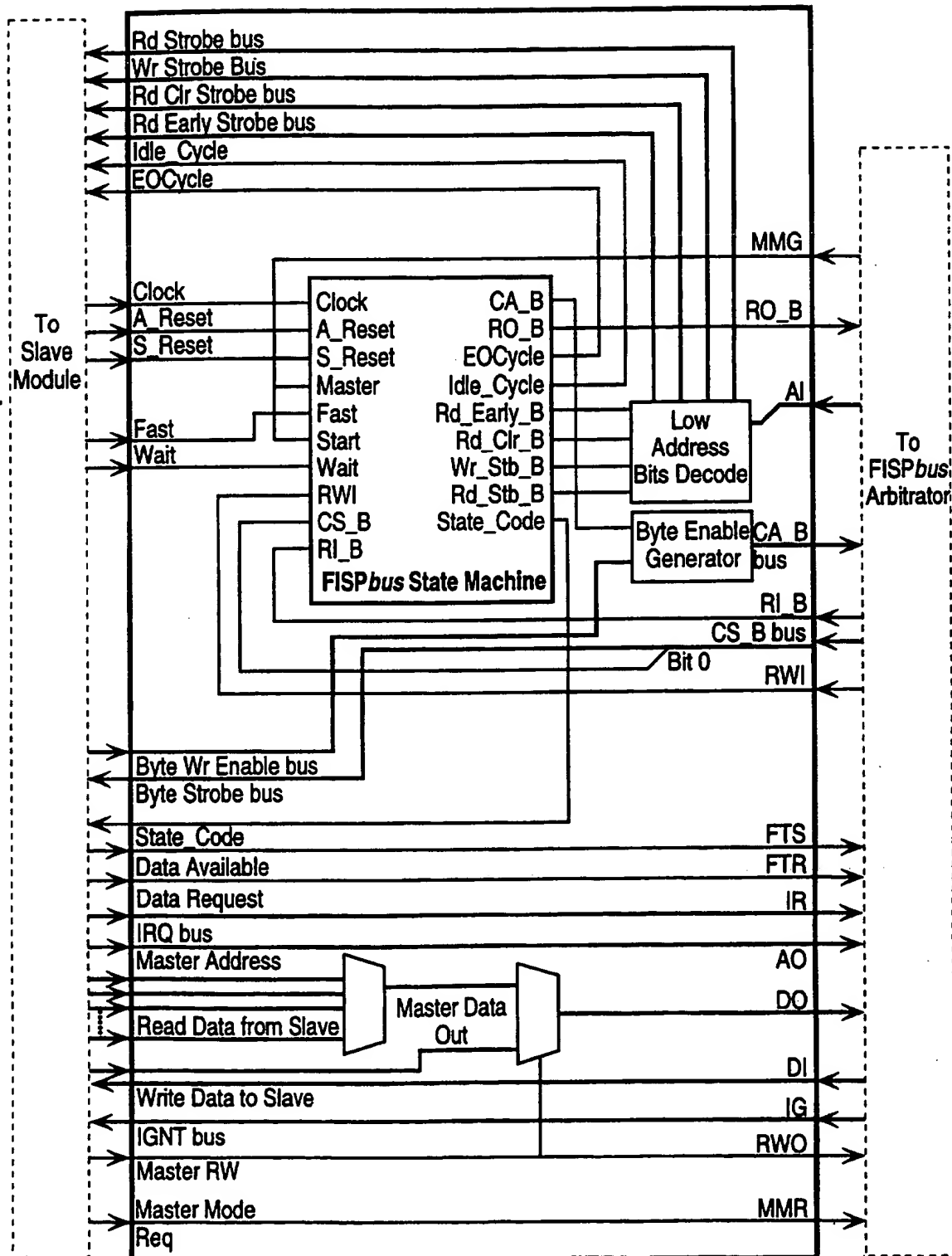


FIG. 24

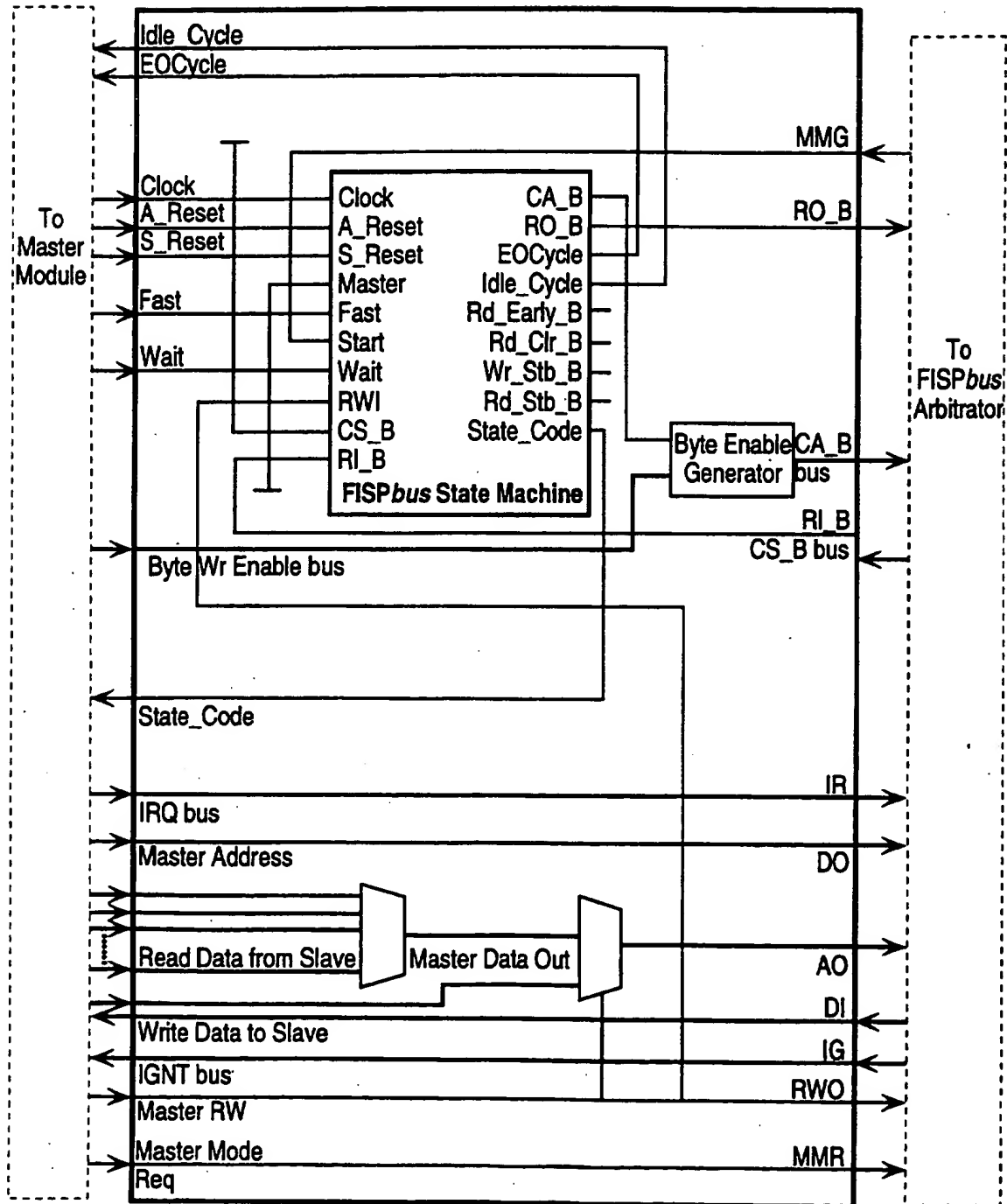


FIG. 25

A Scalable Processor independent On-Chip Bus**BACKGROUND OF THE INVENTION**5 1. **Field of the Invention**

The present invention relates to the field of integrated circuits (IC).
More specifically, the present invention relates to on-chip bus.

10 2. **Background Information**

Computer system designers have long recognized the benefits of
having standardized system buses. Examples of such buses include the S-bus
developed by Sun Microsystems of Mountain View, CA for SPARC based
15 workstations, and Peripheral Component Interface (PCI) bus developed by the PCI
Special Interest Group (SIG) of Hillsboro, OR, for Intel Architecture based personal
computers. In each of these cases, the existence of a standardized system bus
enables numerous interoperable peripherals to be developed by different
manufacturers, enriching the functionality and choices available for the system
20 purchasers.

However, the practice has not been adopted by microprocessor or
application specific integrated circuit (ASIC) designers. Virtually all on-chip buses
known in the art are proprietary, and intended for a specific processor or ASIC
25 family. As time-to-market become increasingly critical, more and more on-chip
function blocks are designed for multiple processor and/or ASIC families. Thus, a
need exists for a scalable processor independent bus.

SUMMARY OF THE INVENTION

A scalable processor independent bus is disclosed. In accordance with one aspect of the present invention, each bus master function block is provided with a bus master interface having a state machine that implements at least two operational modes, including a two state fast mode, and an at least four state normal mode. In accordance with another aspect of the present invention, each bus slave function block is likewise provided with a bus slave interface having a state machine that implements the two operational modes in a complementary manner.

10 In accordance with yet another aspect of the present invention, each bus master/slave function block is provided with a bus master/slave interface having a state machine that implements the at least two operational modes in the role of a bus master as well as in the role of a bus slave.

15 In accordance with yet another aspect of the present invention, in various embodiments of the present invention, each bus master, slave, or master/slave interface is equipped to facilitate scaling of the address as well as data width. Additionally, the bus is equipped to support multiple masters on the bus, broadcast writes, burst mode transfers, and/or tri-states.

20

BRIEF DESCRIPTION OF DRAWINGS

The present invention will be described by way of exemplary embodiments, but not limitations, illustrated in the accompanying drawings in which
5 like references denote similar elements, and in which:

Figure 1 illustrates an integrated circuit incorporated with a basic configuration of the present invention;

Figures 2 - 3 illustrates one embodiment each of the operational states and transitional rules of the state machine incorporated in the bus master and
10 the bus slave interface respectively;

Figures 4 - 6 summarize the basic control signals for facilitating bus transactions;

Figures 7 - 14 are timing diagrams illustrating signal timings for read/write operations between a fast/slow bus master and a fast/slow bus slave;

15 **Figures 15 - 16** summarize additional control signals, including those for facilitating scaling of address and data width;

Figure 17 illustrates another exemplary integrated circuit incorporated with a more complex configuration of the present invention;

Figure 18 illustrates data alignment for one embodiment of the present
20 invention;

Figures 19 - 20 illustrate one embodiment of an arbitrator suitable for use with the present invention;

Figures 21 - 22 illustrate one embodiment of the manner in which burst mode transfer is supported; and

25 **Figure 23 - 25** illustrate one embodiment each of a bus master, a bus slave, and a bus master/slave interface.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, various aspects of the present invention will be described. However, it will be apparent to those skilled in the art that the present invention may be practiced with only some or all aspects of the present invention. For purposes of explanation, specific numbers, materials and configurations are set forth in order to provide a thorough understanding of the present invention. However, it will also be apparent to one skilled in the art that the present invention may be practiced without the specific details. In other instances, well known features are omitted or simplified in order not to obscure the present invention.

Referring now **Figure 1**, wherein a block diagram illustrating an exemplary integrated circuit incorporated with a basic configuration of the present invention is shown. As illustrated, exemplary integrated circuit **100** includes a bus master functional block **102**, a number of bus slave functional blocks **104a**, ... **104n**, and the bus itself **106**, coupled to each other via address decoder **105** as shown. Bus master functional block **102** is equipped with bus master interface **112** incorporated with the teachings of the present invention. Similarly, each bus slave functional block **104a**, ... or **104n** is equipped with a bus slave interface **114** incorporated with the teachings of the present invention. Bus master interface **112** and each bus slave interface **114** interact with each other on behalf of their respective host functional blocks **102**, **104a**, ... and **104n** in accordance with the teachings of the present invention, thereby enabling bus transactions to be conducted among functional blocks **102**, **104a**, ... and **104n** in a processor independent manner. Furthermore, by virtue of the teachings of the present invention incorporated, address and data width may be scaled for different implementations of IC **100**.

In accordance with the teachings of the present invention, each bus master/slave interface 102, 104a, ... or 104n is equipped with a state machine that conducts the bus transactions on behalf of its interface' host functional block in the role of a bus master/slave. Each state machine supports at least two modes of operations, a two state fast mode, and an at least four state normal mode. At any point in time, the bus master functional block may address one or many bus slave functional blocks, depending on the address accessed. **Figures 2 – 3** illustrate the states and the transitional rules implemented by the state machine provided to bus master interface 102, and each of bus slave interface 104a, ... or 104n respectively. **Figures 4 – 6** summarize the basic control signals employed to facilitate conduct of bus transactions.

As shown in **Figure 2**, on RESET the state machine provided to master interface 102 is in the P0 (idle) state. To initiate a cycle, the mode of the required cycle is set using the FAST signal. Once the START signal is asserted, an access cycle begins. The RWI line is driven to indicate the type of access that is required. If the Master is expecting to lengthen the access cycle (for example to ensure that data is held longer on the bus, or if bridging from an asynchronous domain and additional cycles are required to ensure that the data is ready before the actual write operation) then the WAIT line is also held active. The WAIT line is sampled on the rising edge of every clock to create the DWAIT signal.

Once the state machine has seen an active START signal, the access cycle begins. In FAST mode the bus will ignore any WAIT requests (from both the Master and Slave) and directly transition to state P3 (end of cycle). The EOCycle signal will be asserted and on the next clock, the state machine transitions back to

P0, and asserts the IDLE_Cycle signal. The transition to state P3 causes both the CA_B and the RO_B signals to go active simultaneously. These signals are connected to the CS_B and RI_B inputs of the bus slave interface, and indicates to the bus slave that a FAST access is in progress. When not in FAST mode, the state machine transitions to state P1 (wait/readiness determination), and the CA_B signal goes active without the ready out (RO_B).

In state P1, the bus master will examine the ready in signal (RI_B) from the bus slave, and the generated delayed wait (DWAIT). If the bus master is not expected to wait and the bus slave is ready, the state machine transitions to state P2. If the bus slave is not ready, and the bus operation is a read operation, the state machine transitions to SWRD (Slave Waiting on Read). If the bus operation is a write operation, and the bus master needs additional cycles, the state machine transitions to MWWR (Master Waiting on Write). If the bus operation is a read operation, and the bus slave is ready, but the bus master requires extra cycles (WAIT asserted), the state machine will transition to MWRD (Master Waiting on Read). Finally if the bus operation is a write operation, the bus slave is not ready, and the bus master does not require additional cycles, the state machine transitions to SWWR (Slave Waits on Write).

20

If the bus slave is holding the bus up on a read (state SWRD) when the ready from the bus slave (RI_B) is active, the state machine transitions to P2 if the bus master does not require any additional waits, and transitions to MWRD (Master Waiting on Read) if the bus master needs more cycles. If the bus master is not yet ready to write, the state machine transitions to the MWWR (Master Waiting on Writes) state. If the bus master waiting requirement completes, the next state is

25

SWWR (Slave Waiting on Writes), unless the bus slave is also ready. In this case, the next state will be state P2 (ready).

- Once all waits by the bus master and bus slave are satisfied, the
- 5 Master is in the P2 state. In all states where the bus master is ready (i.e. SWWR, P2 and P3), the RO_B line is set to active. This will let the corresponding bus slave know that the bus master is ready. Finally the state machine transitions from state P2 to state P3 on the next clock, and from state P3 to state P0 to complete the access cycle. While in the P3 State, the bus master state machine asserts
- 10 EO_Cycle to indicate that the access cycle is complete. In one embodiment, this signal is used to latch data that is read from the bus slave.

- With no wait states, a normal mode access cycle will take 4 clocks and a fast mode access will take 2 clocks. In the normal mode, both the bus master and
- 15 the bus slave are allowed to insert a variable number of wait states. The bus master is also allowed to switch between the normal and the fast mode during IDLE times (i.e. state P0).

- Referring now to Figure 3, on RESET, the state machine provided to a
- 20 bus slave interface is in the P0 state. The bus slave will wait in this idle condition until the CS_B from the bus master (Master output CA_B) goes active. If the ready in line (RI_B) from the bus master (Master output RO_B) is also active when CS_B is active, the bus slave knows that this is a fast mode access. Accordingly, the state machine transitions directly to state P3. This transition causes an assertion of either
- 25 the RD_Stb_B or the WR_Stb_B strobes, depending on the polarity of the read/write (RWI) line. It should be noted that in fast mode, the bus master ignores the bus

slave's ready line, and therefore the cycle will complete in 2 clock cycles, regardless of the bus slave's actual state.

If the chip select line (CS_B) is detected active by the bus master with
5 the ready line (RI_B) inactive, the bus slave will start a normal 4+ cycle by changing to the P1 State. While the CS_B is asserted, the address and RWI line from the bus master are also stable. The bus slave uses this information to determine whether it can service the access. If it requires additional cycles to complete the operation, it will not assert the ready out (RO_B) line. This is controlled by use of the bus slave's
10 WAIT line (which is reclocked to generate-DWAIT). The Wait line is asserted prior to the transition to state P1, and the bus slave continues to insert waits until the WAIT line is deasserted. The handshake between the ready sent by the bus master and the ready sent by the bus slave determines the length of the access. The transition to state P1 generates two strobes (RD_EARLY and WR_EARLY) which are in turn
15 used to initiate operations prior to actual reception or sending of data. A typical example is using the RD_EARLY strobe to update an interrupt service status prior to dispatching the interrupt status to a microprocessor on chip.

Once in the P1 state, the next transition is determined by the state of
20 readiness of the bus slave and the bus master. In a non-broadcast scenario if both the bus slave and bus master are ready (determined by DWAIT and RI_B), the state machine changes to the P2 state, and asserts the appropriate read (RD_Stb_B) or write (WR_Stb_B) strobe. If the bus master is reading, and not ready while the bus slave does not require additional WAIT states, the bus slave transitions to state
25 MWRD (Master Waiting on Read). The transition causes the assertion of the read (RD_Stb_B) strobe. During a read, if the bus master is ready, and the bus slave requires additional WAIT states (DWAIT active), the bus slave transitions to state

SWRD (Slave Waiting on Read). Similarly in the case where the bus master is writing, the state machine changes to the MWWR (Master Waiting to Write) state if the bus master is not ready, and to the SWWR (Slave Waiting to Write) state if the bus master is ready when the bus slave needs more time.

5

In Broadcast writes, the ready outs all the bus slaves are combined with the Master ready out signal to create a new composite ready in (RI_B) to all the bus slaves. This signal is only active when all bus slaves and the bus master are ready. Any bus slave that is faster than the slowest bus slave assumes that the bus master is slow and waits. This ensures that the bus slaves correctly handle broadcast writes, and the length of the access is determined by the slowest bus slave.

When the bus slave is in the MWWR (Master Waiting to Write) state, the bus slave waits until the ready in (RI_B) line goes active. If additional wait states are required by the bus slave, the bus slave goes to the SWWR (Slave Waiting to Write) state. If no additional waits are required when the ready in is active, the state machine transitions to state P2, and asserts the WR_Stb_B strobe. Similarly, if the state machine is in the SWWR state, and the bus slave waits are complete, the state machine transitions to state P2, and asserts the WR_Stb_B strobe.

When the bus slave is in the SWRD (Slave Waiting on Read) state, the bus slave waits until the DWAIT line goes inactive. If the bus master is not ready by this time, the bus slave goes to the MWRD (Master Waiting on Read) state, and asserts the read strobe (RD_Stb_B) signal. If the bus master is ready (signified by RI_B being active) and DWAIT is inactive, the bus slave transitions to state P2, and

asserts the RD_Stb_B strobe. From the MWRD state, the bus slave waits for the bus master to be ready before transitioning to the P2 state.

When reading in the P2 state, at the next clock, the state machine
5 transitions to the P3 state, and asserts the read clear strobe (RD_Clr_B). While in P3 state, the state machine asserts the EO_Cycle. At the next and final clock, the state machine returns to state P0, i.e. the IDLE condition.

Before we continue with the description, it should be note that in fast
10 mode, no facility to delay an access is provided. It is the bus master's responsibility to know that the bus slaves accessed in the fast mode, fully supports fast mode accesses. Thus, functional blocks supporting only a subset of accesses at the fast rate must clearly identify these addresses. It is the responsibility of the system designer then to ensure that these operations are possible.

15 Additionally, in practice, the bus master and the bus slave interfaces are provided with the same state machine, the state machine can switch between acting as a bus master state machine or a bus slave state machine in state P0. In other words, it is possible for a functional block to be a bus master in one point in
20 time, and a bus slave in another point in time.

Figures 7 – 14 illustrate signal timings for read/write operations between a fast/slow bus master and a fast/slow bus slave. More specifically, **Figure 7** illustrates the timing of the above described signals, when a bus master using the
25 two state fast mode to perform either a read or a write operation against a bus slave. **Figure 8** illustrates the timing of the above described signals, when a non-waiting bus master using the at least four state normal mode to perform either a

read or a write operation against a non-waiting bus slave. The read/write operation is completed in four cycles, without using any wait states. **Figures 9 – 10** illustrate the timing of the above described signals, when a fast bus master using the at least four state mode to perform a read and a write operation respectively against a slow bus slave. Three wait states are employed. The required period of wait is determined by the length of the bus slave's WAIT line. **Figures 11 – 12** illustrate the timing of the above described signals, when a slow bus master using the at least four state mode to perform a read and a write operation respectively against a fast bus slave. Again, three wait states are employed. The required period of wait is determined by the length of the bus master's WAIT line. Finally, **Figures 13 – 14** illustrate the timing of the above described signals, when a slow bus master using the at least four state mode to perform a write and a read operation respectively against a slow bus slave. In **Figure 13**, the bus master required 3 wait states, while the bus slave required 4 wait states. In **Figure 14**, the bus master required 4 wait states, while the bus slave required 3 wait states instead.

Referring now to **Figures 15 – 16**, wherein additional control signals, including those for facilitating scaling of address and data width are summarized. As shown, these additional control signals include control signals MMG and MMR for supporting bus grant and bus request, control signals CS_B and CA_B for chip-select, and control signals FTS and FTR for denoting a "free state" to send and receive signal. Furthermore, these control signals include control signal AI for denoting the maximum address range required by the bus slave functional blocks, and control signals DO and DI for denoting the maximum data range required by the bus slaves on the bus. Finally, in some embodiment, the additional control signals also include IG and IR for supporting interrupt handling (to be described more fully below).

Referring now to **Figure 17**, wherein a block diagram illustrating another exemplary integrated circuit incorporated with a more complex configuration of the present invention is shown. As shown, exemplary integrated circuit **200** includes multiple bus master functional blocks **202a – 202b** as well as multiple slave functional blocks **204a – 204c**. Additionally, exemplary integrated circuit **200** includes multiple bus master/slave functional blocks **208a – 208b**, i.e. these functional blocks may be bus masters in certain points in time, and bus slaves in other points in time. One of these exemplary bus master/slave functional block is bus bridge **208a** for bridging to another scalable processor independent bus of the present invention. Another one of these exemplary bus master/slave functional block is processor personality module **208b** where mapping to the unique requirements for processor **212** is handled. Lastly, with the presence of multiple bus master functional blocks, exemplary integrated circuit **200** also includes bus arbitrator **210**. These elements are coupled to each other as shown. As described earlier, each of the bus master, bus slave and bus master/slave functional blocks is provided with a bus master, a bus slave, or a bus master/slave interface of the present invention. Bus arbiter **210** includes address decoder **105** of **Fig. 1**.

Byte Alignment

Referring now to **Figure 18**, wherein a block diagram illustrating the byte alignment approach employed by one embodiment of the present invention is shown. As illustrated, the embodiment implements right aligned transfers of bytes, long words and words. The bottom data bits (7-0) are used for the least significant byte and the highest bits are used for the most significant byte. The right alignment approach removes the endian mode dependency from the functional blocks, allowing functional blocks with different minimum data width requirements to be

easily interfaced. The required endian mode is handled in the corresponding processor personality functional blocks of the different processors. In alternate embodiments, a processor's natural byte orientation may be used instead. In such a situation, the alignment mode used should be clearly documented.

5

Arbitration

Referring now to **Figures 19 – 20**, wherein a block diagram and a waveform diagram illustrate one embodiment of an arbitrator suitable for use with the present invention are shown. As shown in **Figure 19**, for the illustrated
10 embodiment, arbitrator 300 includes arbitration logic 302, a number of multiplexors 304, and a number of AND logic 306. Arbitration logic 302 determines who's the current master. Multiplexors 304 select the appropriate chip select, address and data lines etc. AND logic 306 perform logical AND on the EOCycle and the RO_B signals.

15

The method used by arbitration logic 302 to determine the next master is application dependant, but all logic to determine the next master should be stable within one clock to guarantee that no cycles are lost due to the arbitration process. If this is not possible, the overall bus bandwidth will have to be reduced and the
20 arbiter will have to use some additional clock cycles between bus accesses.

For the illustrated embodiment, the arbitration scheme works by the use of a minimum of two signals. Any master wanting to take bus ownership asserts its MMR signal and requests service from the arbiter. When the arbiter wants to
25 give a master ownership of the bus, it does so by setting the appropriate grant (MMG) line. The MMG signal is used by the bus master to start an access on the bus. When the arbiter detects an end of cycle (EOCycle) from the bus master, it

determines the next master and grants that master ownership of bus for the next access via the MMG line.

5 There are no specific rules as to how the arbiter determines the next master, and it is expected that each application will probably need a different implementation. Examples of previous types of arbitration schemes include priority based, round robin, demand driven and bursty. Various signals on the bus allow the arbiter to decide on the next master including the target addresses, slave FTS, FTR signals. In addition to support bursty transfers the arbiter can allow a single master
10 to occupy contiguous access slots on the bus. In addition to master requests from the bus masters, the arbiter can also receive and send bus requests to and from other arbiter units on secondary buses allowing functional blocks to communicate between different buses via a bus bridge which allows direct connection between two buses under arbiter control.

15

For the illustrated embodiment, the arbitration logic also include address decoding for generating the chip selects to each bus slave as well as address and data multiplexing to put the current master's information on the bus. The arbiter also generates the ready in lines for each of the masters by anding all
20 the ready lines from the slave units.

The waveform diagram shows a fast Master (Master 1) and a normal 4 cycle master (Master 2) both requesting bus mastership from the arbiter. Master 2 is given first access and completes. The end of cycle signal from Master 2 enables
25 the arbiter to choose Master 1 as the next master and bus ownership is then handed to Master 1. The arbitration is conducted during the previous cycles end of cycle period and therefore does not result in any additional clock cycles for bus arbitration.

If additional time is taken to arbitrate the bus and the grant (MMG) is delayed additional idle (P0) states will be added.

Interrupt Handling

- 5 In one embodiment, the scalar processor independent bus of the present invention also supports both vectored and non vectored interrupts. The generation of the vector from an interrupt is the function of the appropriate microprocessor personality functional block. As described earlier, each functional block with a bus interface incorporated with the teachings of the present invention
- 10 has two signals defined for interrupt support IG and IR. These signals are busses with the width matching the number of interrupts that are present in the functional block + 1. The extra signal is bit 0 of the interrupt lines, and is defined as the AND of all the functional block interrupt requests (IR) or interrupt Grants (IG).
- 15 It is not mandatory for a functional block to fully support vectored interrupts. In this case bit 0 of the IR bus is driven and all other bits of the IR and IG are ignored. The documentation for the functional block should clearly state whether support for vectored interrupts is provided.
- 20 In a number of embodiments, support for vectored interrupts is provided in the microprocessor personality functional block (MPFB). The various IR buses from each functional block is fed back to the microprocessor personality functional block. Any interrupts requiring vector support are used to drive a vector look up table and the appropriate vector is returned to the microprocessor. When
- 25 the acknowledgement is received from the microprocessor, the appropriate IG bit is driven to clear the interrupt down.

Asynchronous Interfacing

In one embodiment, the scalar processor independent bus is a fully synchronous on-chip bus system. However, when interfacing to microprocessors and designing systems it is inevitable that certain functional blocks will need to run
5 asynchronously to the bus. The basic method is to generate a clean (i.e. re-clocked) signal to drive the WAIT input to the bus interface state machine.

For example, in an asynchronous bus slave interface, some read and write registers will need to be in the bus slave's clock domain, while the bus slave
10 interface is in the bus' clock domain. In such cases, the resultant read and write strobes can be extended for additional clocks with new circuitry, and then re-synchronised to the bus slave's clock domain. Once this is complete, the resultant strobe signal should also be used to inhibit the extension of the bus cycle. All read data should be latched from the bus slave's clock domain into the bus' clock domain
15 before any read cycles are terminated. By using the state code of the bus interface's state machine and the status of the extended strobes, the bus can be made to wait until the access is successfully completed. The WAIT pin is used to ensure that the bus access is extended until the synchronisation process is complete.

20

The WAIT input must be synchronous and if necessary has to be retimed to ensure that metastability conditions are handled correctly. The ability to add wait states to both the master and slave interfaces allows it to easily interface to asynchronous clock domains by simply extending the bus cycle as required.

25

Broadcast Write Accesses

In one embodiment, Broadcast accesses are implicitly supported through the arbitration mechanism. It is expected that the broadcast access facility will be used for specific registers or banks of bus masters/slaves all expected to be used in the same manner. Care must be taken in the design of the arbiter to ensure
5 that the broadcast accesses are restricted to write accesses only.

If the bus is used in fast mode, the system designer must ensure that all the broadcast slaves are capable of 2 cycle access. In this mode, no wait or other support is provided for ensuring that the broadcast access has been
10 successfully completed, and it relies on correct operation by virtue of the design. The ability of each slave to deassert the free to receive (FTR) line can provide additional information to the arbiter to ensure that all the relevant slaves are capable of taking the next broadcast access. When using the FTR line to control accesses, the length of contiguous accesses will be limited by the slave with the smallest
15 buffer capacity (i.e. by the first slave to deassert FTR). Any bus slave location supporting fast accesses by default supports broadcast bursts writes, if this register also controls the FTR line.

The general operation of the 4+ cycle depends on the ready out
20 (RO_B) and ready in (RI_B) lines to both the master and slave interfaces. In non broadcast accesses the ready in to the bus master is the ready out from the addressed slave. In broadcast accesses the ready in to the slaves is made by ANDING all the active low ready out lines from all addressed slaves as well as the ready out from the bus master. This would cause the period of any access cycle to
25 be extended to accommodate the slowest slave. The bus master ready in is made by ANDING all the active low ready out lines from all the addressed slaves. In practice, this selective ANDING of the ready lines is undertaken in the arbiter unit.

Burst Mode Accesses

Burst Mode accesses can only be initiated by a bus master that supports Burst Mode accesses and Slave registers that support fast (2 cycle) accesses or Slave registers that support Burst Mode accesses. Any bus master/slave that supports burst mode transfers must explicitly define the registers that support this mode and the expected method of operation.

Burst mode accesses can only be used when addressing contiguous ascending address locations (i.e. N, N+1, N+2 N+M) and while continuously reading or writing. Various parts of the interface control the length and operation of burst mode transfers. The length of the burst source can be any length and this is defined by the bus master. The length of burst that a slave can take is determined by the slave. The arbiter determines the length of the continuous burst that a particular master is allowed to have.

To facilitate the Burst Mode two additional control lines (BA_B - Burst Active and OK2B – OK to burst) are used. The BA_B signal is generated by a burst supporting master and the current masters BA_B signal is channelled to the slave. On the master and slave entities, the BA_B signal is usually represented as BAO_B for the master and the BAI_B for the slave. The OK2B signal is generated by the slave and provides indication to the bus arbiter that the slave can now sustain burst transfers. The BA_B line is used to signify that the current access is part of a burst transfer. This allows a burst mode compatible bus slave to get ready for the burst transfer. Generally, the slave will pre-fetch information or undertake certain tasks in preparation for the burst. The time available to undertake this is determined by the

bus slave. However, once the first access is complete, the burst transfer protocol expects all other transfers to take place at a fast 2-cycle rate.

5 The basic bus operation is not changed during this mode but a higher level protocol is employed. The burst starts with a 4+ cycle access and all subsequent accesses from the bus master are in fast mode (2 cycles). The bus master asserts the active low Burst Active line (BAO_B) on its transition from state P0 to P1 and deasserts BAO_B after the final 2 cycle transfer during the state change from P3 to P0. At the slave end, the start and subsequent burst accesses
10 are signalled by the BAI_B input line being active during P0. If the BAI_B is inactive during P3 of the bus slave, an end of burst sequence is signalled. A new burst transfer may then be signalled by the BAI_B being set again at P0, and a new 4+ cycle will start.

15 The bus slave can extend the first cycle by using the WAIT control and can terminate the burst transfers by signalling to the arbiter that the ability to receive or send data is over. This is facilitated by removing the OK to burst signal (OK2B). The arbiter allows a master to burst transfer by granting the master bus ownership for more than one access cycle. The bus master will start the transfer when it first
20 gets the grant, and continues to burst until the master mode grant line (MMG) goes inactive or the bus master has completed the burst.

Figures 21 – 22 illustrate how the standard master mode control signals of the bus interface state machine are controlled in bus master interfaces
25 that support the burst transfer mode. This state machine must be added to any bus master circuit that supports the burst transfer mode. On the bus slave interface, the bus slave has to examine the burst active input (BAI_B) line to determine if a burst

transfer is occurring. Multiple bus masters are allowed to burst to the same slave by
banding the BAO_B lines together and generating the final BA_B signal. The state
machine described above ensures that between burst transfers the BA_B line will be
inactive during master state P0. The bus slave examines the initial burst status
5 during its P0, but will examine the continuing burst status during its state P3.

Tristate Architectures

So far, the present invention has been described as using multiplexers
and separate data in and data out lines. This is preferred as it allows the bus
10 master/slave interfaces to be used on any ASIC process. However, there are
sometimes system requirements for using a tristate bus.

The structure of the present invention has ensured that the bus
direction control is concentrated in the arbiter. In the descriptions presented, the
15 direction control is provided by multiplexers. In a tristate implementation tristate
drivers will need to be added to the data lines and the master address lines. The
arbiter will then have to be modified to generate appropriate control signals to
control these signals. In addition, the ready out lines (RO_B) and burst active
(BA_B) lines can also be made tristate. Care must be taken to ensure that when no
20 bus master is active, the bus lines are driven to inactive or default states (as
appropriate).

Error Control

In systems where all the addresses are not fully decoded there is a
25 possibility for the bus to access a non existent peripheral and hang, waiting for a
ready that never arrives. In one embodiment, a watchdog timer (the length of which
is determined by the application) is added to the system to reset the bus if this

situation arises. In another embodiment, all addresses are ensured to be always fully decoded, and the bus slaves exist at all addresses.


Finally, **Figure 23 - 25** illustrate one embodiment each of a bus master, a bus slave, and a bus master/slave interface. Shown in **Figure 23** is an exemplary bus slave module. As mentioned previously the bus master and Slave state machines are implemented using the same logic. The Master, Fast and Start control signals on this machine are only used during the master mode and are therefore tied off to an active high value when used in a bus slave. **Figure 24** illustrated the structure of a combined bus master and slave interface. The additional signals required to support bus master interfaces were described earlier. Lastly, **Figure 25** the host and bus connections that are required to implement a bus master interface. The bus master has some additional control signals for control of the bus arbitration process.

15

Thus, a scalable processor independent on-chip bus has been described. While the method and apparatus of the present invention has been described in terms of the above illustrated embodiments, those skilled in the art will recognize that the invention is not limited to the embodiments described. The present invention can be practiced with modification and alteration within the spirit and scope of the appended claims. The description is thus to be regarded as illustrative instead of restrictive on the present invention.

CLAIMS

1. An integrated circuit comprising a bus, a first bus master function block coupled to the bus, and a slave function block also coupled to the bus, the first bus master function block having a bus master interface including a state machine that conducts a bus transaction between the first bus master function block and the bus slave function block in either a two state fast mode of operation, or an at least four state normal mode of operation, wherein the at least four states of the at least four state normal mode of operation includes the two states of the two state fast mode of operation.
2. The integrated circuit of claim 1, wherein the at least four state normal mode of operation comprises an idle state, a wait/readiness determination state, a ready state and an end of cycle state, and the two state fast mode of operation consists the idle state and the end of cycle state.
3. The integrated circuit of claim 2, wherein the at least four state normal mode of operation further comprises one or more of a slave waiting on read (SWRD) state, a master waiting on read (MWRD) state, a master waiting on write (MWWR) state and a slave waiting on write (SWWR) state.
4. The integrated circuit of claim 2, wherein the state machine includes transition logic for transitioning the bus master interface from the idle state to the



wait/readiness determination state if a mode signal denotes the at least four state normal mode of operation, otherwise, to the end of cycle state.

5. The integrated circuit of claim 4, wherein the state machine further includes transition logic for automatically transitioning the bus master interface from the end of cycle state to the idle state after one clock cycle.

6. The integrated circuit of claim 4, wherein the state machine further includes transition logic for transitioning the bus master interface from the wait/readiness determination state to a slave waiting on read (SWRD) state if the slave function block is not ready and the bus transaction is a read operation.

7. The integrated circuit of claim 4, wherein the state machine further includes transition logic for transitioning the bus master interface from the wait/readiness determination state to a master waiting on write (MWWR) state if the first master function block is not ready and the bus transaction is a write operation.

8. The integrated circuit of claim 4, wherein the state machine further includes transition logic for transitioning the bus master interface from the wait/readiness determination state to a slave waiting on write (SWWR) state if the slave function block is not ready and the bus transaction is a write operation.

9. The integrated circuit of claim 4, wherein the state machine further includes transition logic for transitioning the bus master interface from the wait/readiness determination state to a master waiting on read (MWRD) state if the first master function block is not ready and the bus transaction is a read operation.

10. The integrated circuit of claim 4, wherein the state machine further includes transition logic for transitioning the bus master interface from either the wait/readiness determination state, a slave waiting on read (SWRD) state, a master waiting on write (MWWR) state, a slave waiting on write (SWWR) state, or master waiting on read (MWRD) state to the ready state if either no waiting is required or required waiting has occurred.

11. The integrated circuit of claim 1, wherein the integrated circuit further includes a second bus master function block also coupled to the bus and having a like bus master interface, and an arbitration unit also coupled to the bus for arbitrating access to the bus between the first and second master function block.

12. The integrated circuit of claim 1, wherein the first bus master function block is a microprocessor personality block, and the integrated circuit further includes a microprocessor coupled to the first master function block.

13. The integrated circuit of claim 1, wherein the bus master interface is further equipped to burst transfer data to the slave function block.

14. An integrated circuit comprising a bus, a first bus master function block coupled to the bus, and a bus slave function block also coupled to the bus, the bus slave function block having a bus slave interface including a state machine that conducts a bus transaction between the first bus master function block and the bus slave function block in either a two state fast mode of operation, or an at least four state normal mode of operation, wherein the four states of the at least four state normal mode of operation includes the two states of the two state fast mode of operation.

15. The integrated circuit of claim 14, wherein the at least four state normal mode of operation comprises an idle state, a wait/readiness determination state, a ready state and an end of cycle state, and the two state fast mode of operation consists the idle state and the end of cycle state.

16. The integrated circuit of claim 15, wherein the at least four state normal mode of operation further comprises one or more of a slave waiting on read (SWRD) state, a master waiting on read (MWRD) state, a master waiting on write (MWWR) state and a slave waiting on write (SWWR) state.

17. The integrated circuit of claim 15, wherein the state machine includes transition logic for transitioning the bus slave interface from the idle state to the wait/readiness determination state if a mode signal denotes the at least four state normal mode of operation, otherwise, to the end of cycle state.

18. The integrated circuit of claim 17, wherein the state machine further includes transition logic for automatically transitioning the bus slave interface from the end of cycle state to the idle state after one clock cycle.

19. The integrated circuit of claim 17, wherein the state machine further includes transition logic for transitioning the bus slave interface from the wait/readiness determination state to a slave waiting on read (SWRD) state if the slave function block is not ready and the bus transaction is a read operation.

20. The integrated circuit of claim 17, wherein the state machine further includes transition logic for transitioning the bus slave interface from the wait/readiness

determination state to a master waiting on write (MWWR) state if the first master function block is not ready and the bus transaction is a write operation.

21. The integrated circuit of claim 17, wherein the state machine further includes transition logic for transitioning the bus slave interface from the wait/readiness determination state to a slave waiting on write (SWWR) state if the slave function block is not ready and the bus transaction is a write operation.

22. The integrated circuit of claim 17, wherein the state machine further includes transition logic for transitioning the bus master interface from the wait/readiness determination state to a master waiting on read (MWRD) state if the first master function block is not ready and the bus transaction is a read operation.

23. The integrated circuit of claim 17, wherein the state machine further includes transition logic for transitioning the bus slave interface from either the wait/readiness determination state, a slave waiting on read (SWRD) state, a master waiting on write (MWWR) state, a slave waiting on write (SWWR) state, or master waiting on read (MWRD) state to the ready state if either no waiting is required or required waiting has occurred.

24. The integrated circuit of claim 14, wherein the integrated circuit further includes a second bus master function block also coupled to the bus, and an arbitration unit also coupled to the bus for arbitrating access to the bus between the first and second master function blocks.

25. The integrated circuit of claim 14, wherein the first bus master function block is a microprocessor personality block, and the integrated circuit further includes a microprocessor coupled to the first master function block.

26. The integrated circuit of claim 14, wherein the bus slave interface is further equipped to receive burst transferred data from the first master function block.

27. An integrated circuit comprising a bus, a bus master/slave function block coupled to the bus, and either a bus master or a bus slave function block also coupled to the bus, the bus master/slave function block having a bus master/slave interface including a state machine that conducts a bus transaction with the bus master or slave function block as a bus master if the bus master or slave function block is a bus slave function block or as a bus slave if the bus master or slave function block is a bus master function block, the bus transaction being conducted in either a two state fast mode of operation, or an at least four state normal mode of operation, wherein the four states of the at least four state normal mode of operation includes the two states of the two state fast mode of operation.

28. The integrated circuit of claim 27, wherein the at least four state normal mode of operation comprises an idle state, a wait/readiness determination state, a ready state and an end of cycle state, and the two state fast mode of operation consists the idle state and the end of cycle state.

29. The integrated circuit of claim 28, wherein the at least four state normal mode of operation further comprises one or more of a slave waiting on read (SWRD) state, a master waiting on read (MWRD) state, a master waiting on write (MWWR) state and a slave waiting on write (SWWR) state.

30. An integrated circuit comprising:

a bus;

a bus master function block coupled to the bus, the bus master function block having a bus master interface including a state machine that implements a two state fast mode of operation, and a at least four state normal mode of operation, wherein the four states of the at least four state normal mode of operation includes the two states of the two state fast mode of operation; and

a bus slave function block coupled to the bus, the bus slave function block having a bus slave interface including a state machine that implements in a complementary manner the two state fast mode of bus operation, and the at least four state normal mode of operation.

31. The integrated circuit of 30; wherein the integrated circuit further includes a bus master/slave function block coupled to the bus, the bus master/slave function block having a bus master/slave interface including a state machine that implements in a complementary manner the two state fast mode of operation, and the at least four state normal mode of operation.

32. The integrated circuit of 30; wherein the integrated circuit further includes another bus master function block coupled to the bus, the other bus master function also having a bus master interface including a state machine that implements the two state fast mode of bus operation, and the at least four state normal mode of operation; and

an arbiter coupled to the bus for arbitrating bus accesses for the bus master function blocks.

33. An integrated circuit comprising a bus, substantially as hereinbefore described with reference to the accompanying drawings,